PRODUCT SUMMARY (TYPICAL)	
V_{DS} (V)	600
$R_{DS(on)}$ (mΩ)	52
Q_{rr} (nC)	127

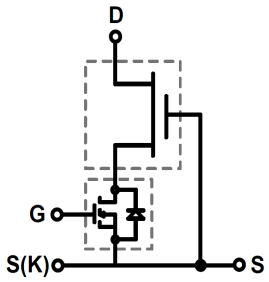
GaN Power Low-loss Switch

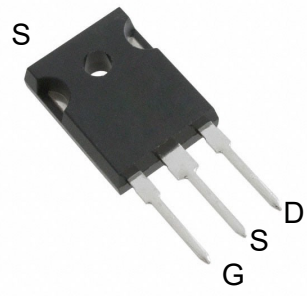
Features

- Low Q_{rr}
- Free-wheeling diode not required
- Quiet Tab™ for reduced EMI at high dv/dt
- GSD pin layout improves high speed design
- RoHS compliant
- High frequency operation

Applications

- Compact DC-DC converters
- AC motor drives
- Battery chargers
- Switch mode power supplies





TO-247 3L Package

Absolute Maximum Ratings (T_C=25 °C unless otherwise stated)

Symbol	Parameter		Limit Value	Unit
$I_{D25°C}$	Continuous Drain Current @T_C=25 °C		36	A
$I_{D100°C}$	Continuous Drain Current @T_C=100 °C		25	A
I_{DM}	Pulsed Drain Current (pulse width:10 μs)		150	A
V_{DSS}	Drain to Source Voltage		600	V
V_{TDS}	Transient Drain to Source Voltage [a]		750	V
V_{GSS}	Gate to Source Voltage		±18	V
$P_{D25°C}$	Maximum Power Dissipation		150	W
T_C	Operating Temperature	Case	-55 to 150	°C
T_J		Junction	-55 to 175	°C
T_S	Storage Temperature		-55 to 150	°C
T_{Csold}	Soldering peak Temperature [b]		260	°C

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\Theta JC}$	Junction-to-Case	1.0	°C /W
$R_{\Theta JA}$	Junction-to-Ambient	40	°C /W

Notes

a: In off state, spike duty cycle D<0.1, duration <1us

b: For 10 sec, 1.6mm from the case

Electrical Characteristics (T_C=25 °C unless otherwise stated)

Symbol	Parameter	Min	Typical	Max	Unit	Test Conditions
Static						
$V_{DSS-MAX}$	Maximum Drain-Source Voltage	600	-	-	V	V_{GS}=0 V
$V_{GS(th)}$	Gate Threshold Voltage	1.6	2.1	2.6	V	V_{DS}=V_{GS}, I_D=0.7mA
$R_{DS(on)}$	Drain-Source On-Resistance (T_J = 25 °C)	-	52	63	mΩ	V_{GS}=8V, I_D =24A, T_J = 25 °C
$R_{DS(on)}$	Drain-Source On-Resistance (T_J = 175 °C)	-	120	-	mΩ	V_{GS}=8V, I_D =24A,T_J = 175 °C
I_{DSS}	Drain-to-Source Leakage Current, T_J = 25 °C	-	4	40	μA	V_{DS}=600V, V_{GS}=0V, T_J = 25 °C
I_{DSS}	Drain-to-Source Leakage Current, T_J = 150 °C	-	40	-	μA	V_{DS}=600V, V_{GS}=0V, T_J = 150 °C
I_{GSS}	Gate-to-Source Forward Leakage Current	-	-	400	nA	V_{GS}= 18 V
	Gate-to-Source Reverse Leakage Current	-	-	-400		V_{GS}= -18 V
Dynamic						
C_{ISS}	Input Capacitance	-	1157	-	pF	V_{GS}=0 V, V_{DS}=400 V, *f* =1 MHz
C_{OSS}	Output Capacitance	-	124	-		
C_{RSS}	Reverse Transfer Capacitance	-	11.9	-		
$C_{O(er)}$	Output Capacitance, energy related [a]	-	178	-		V_{GS}=0 V, V_{DS}=0 V to 400 V
$C_{O(tr)}$	Output Capacitance, time related [b]	-	293	-		
Q_g	Total Gate Charge	-	28	42	nC	V_{DS} =400 V, V_{GS}= 0-8V, I_D = 24 A
Q_{gs}	Gate-Source Charge	-	10	-		
Q_{gd}	Gate-Drain Charge	-	6	-		
$t_{d(on)}$	Turn-On Delay	-	22	-	ns	V_{DS} =480 V , V_{GS}= 0-10 V, I_D = 24 A, R_G = 2Ω
t_r	Rise Time	-	7.5	-		
$T_{d(off)}$	Turn-Off Delay	-	33	-		
t_f	Fall Time	-	4.5	-		
Reverse operation						
I_S	Reverse Current	-	-	25	A	V_{GS}=0 V, T_C=100 °C
V_{SD}	Reverse Voltage	-	1.8	2.4	V	V_{GS}=0 V, I_S=24 A, T_J=25 °C
V_{SD}	Reverse Voltage	-	1.25	1.5	V	V_{GS}=0 V, I_S=12 A, T_J=25 °C
t_{rr}	Reverse Recovery Time	-	30	-	ns	I_S=24 A, V_{DD}=400 V, di/dt =1000A/μs, T_J=25 °C
Q_{rr}	Reverse Recovery Charge	-	127	-	nC	

Notes
a: Equivalent capacitance to give same stored energy from 0 to 400V
b: Equivalent capacitance to give same charging time from 0 to 400V

Typical Characteristic Curves 25 °C unless otherwise noted

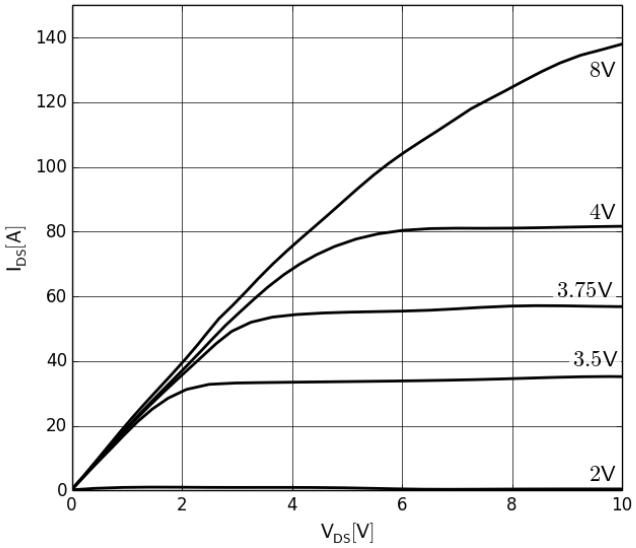


Fig. 1. Typical Output Characteristics T_J= 25 °C
Parameter: V_{GS}

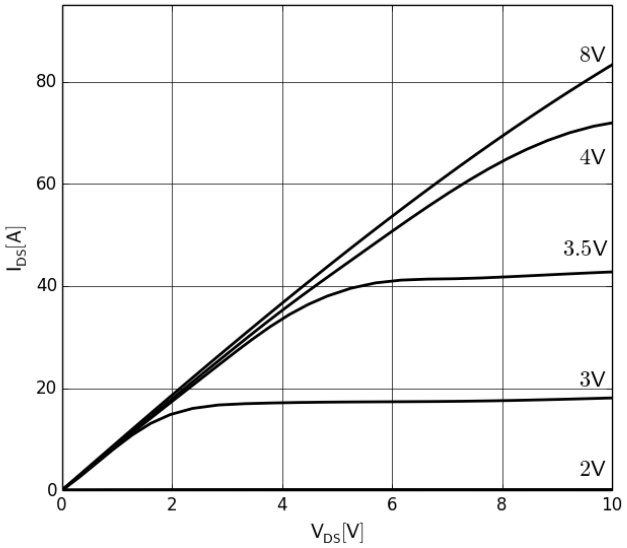


Fig. 2. Typical Output Characteristics T_J=175 °C
Parameter: V_{GS}

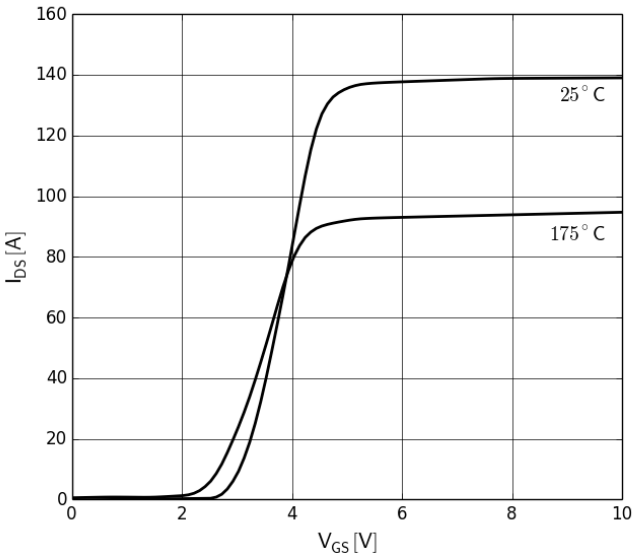


Fig. 3. Typical Transfer Characteristics
V_{DS}=10 V, Parameter: T_J

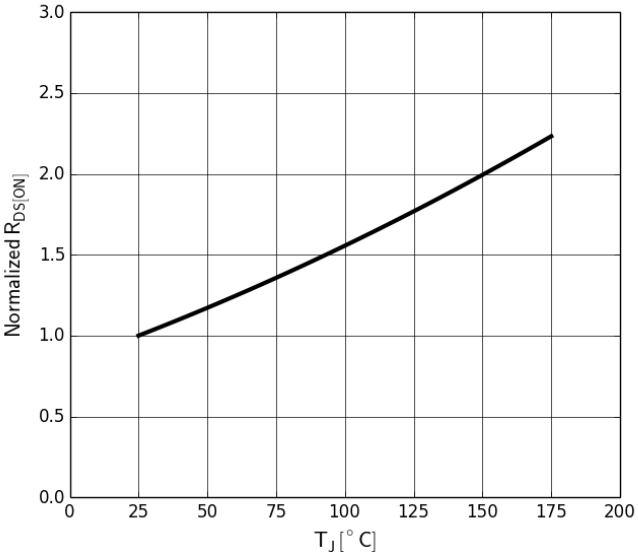


Fig. 4. Normalized On-Resistance
I_D=12 A, V_{GS}=8 V

Typical Characteristic Curves 25 °C unless otherwise noted

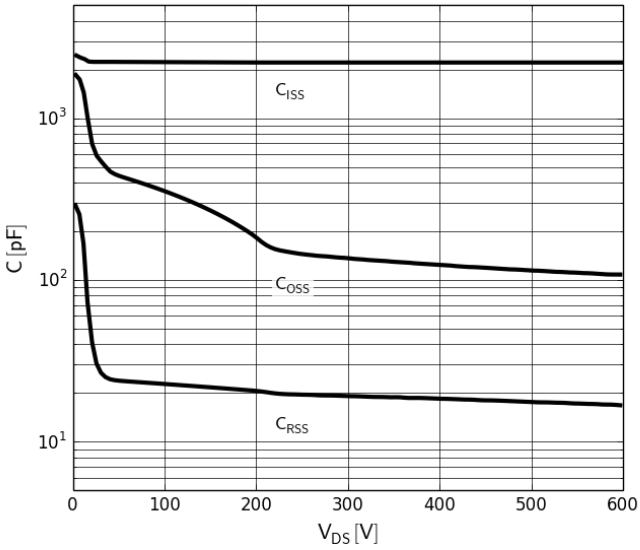


Fig. 5. Typical Capacitance
V_{GS}=0 V, f=1 MHz

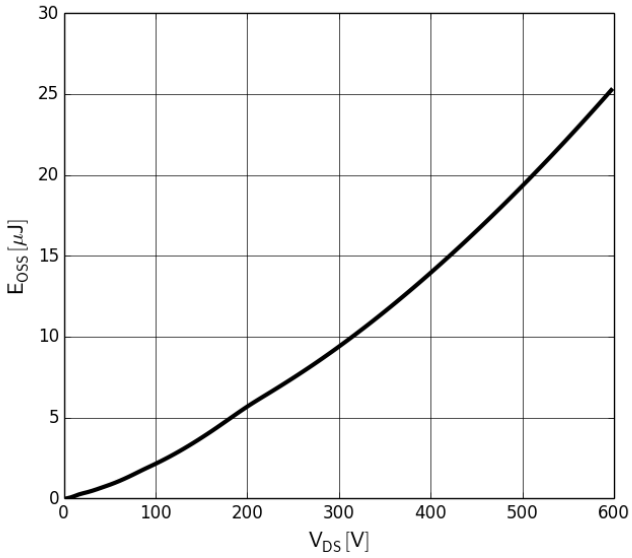


Fig. 6. Typical C_{oss} Stored Energy

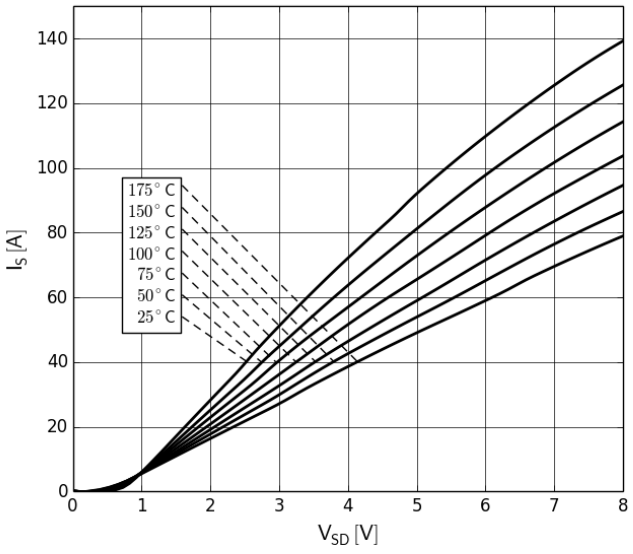


Fig. 7. Forward Characteristics of Rev. Diode
I_S=f(V_{SD}); parameter Tj

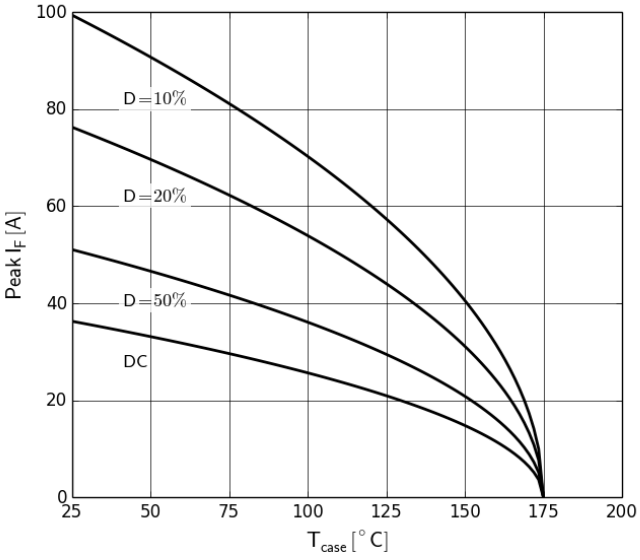


Fig. 8. Current Derating
Pulse Width = 100µs

Typical Characteristic Curves 25 °C unless otherwise noted

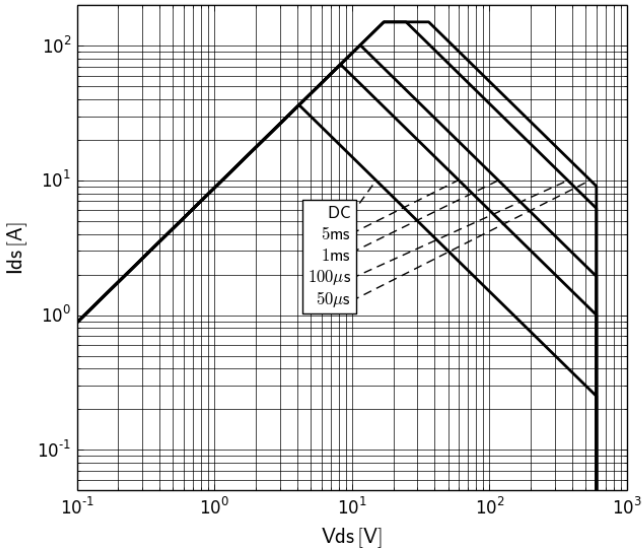


Fig. 9. Safe Operating Area T_C = 25 °C

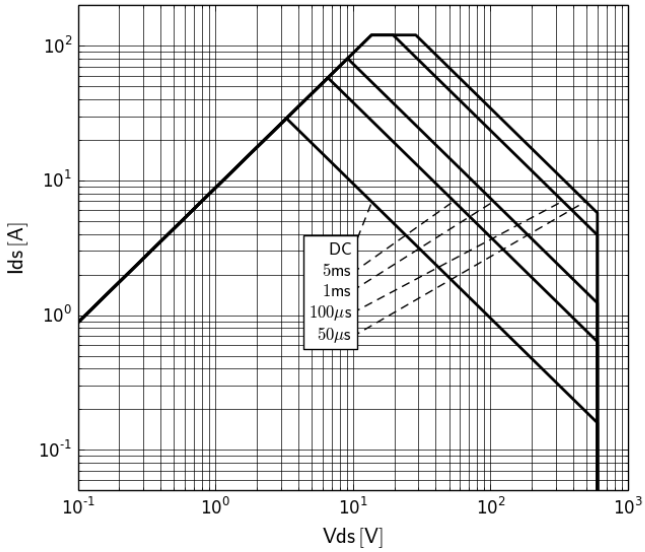


Fig. 10. Safe Operating Area T_C = 80 °C

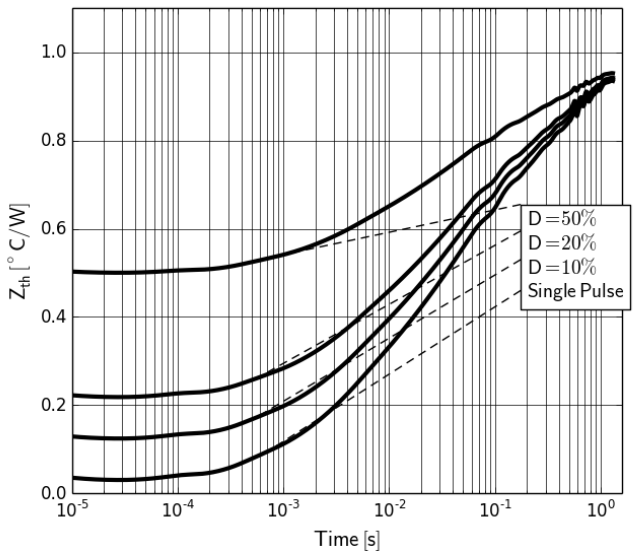


Fig. 11. Transient Thermal Resistance

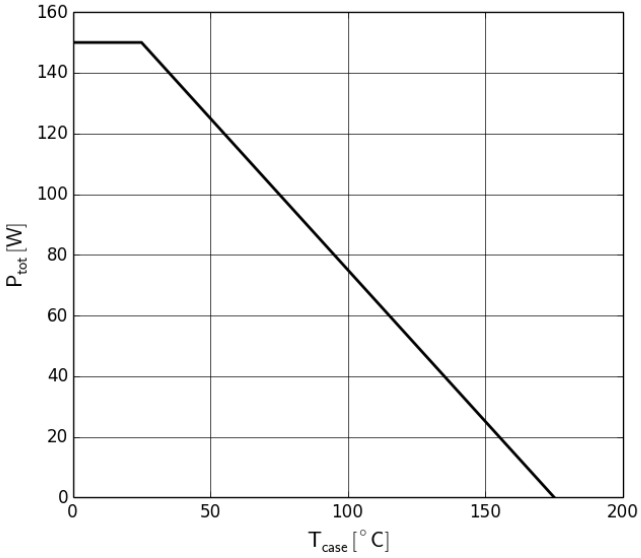


Fig. 12. Power Dissipation

Test Circuits and Waveforms

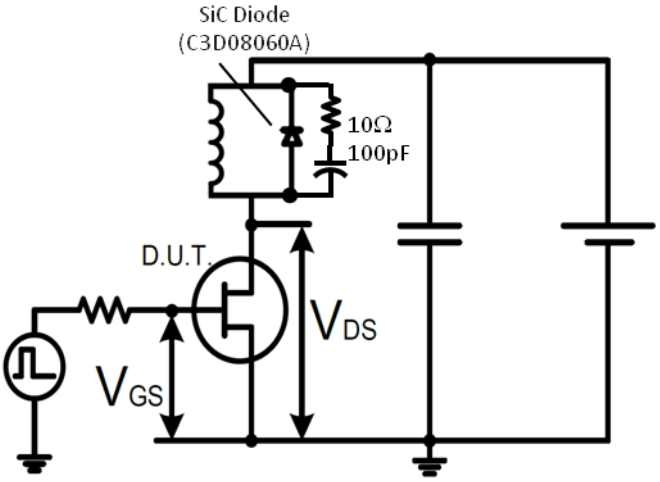


Fig. 1. Switching Time Test Circuit

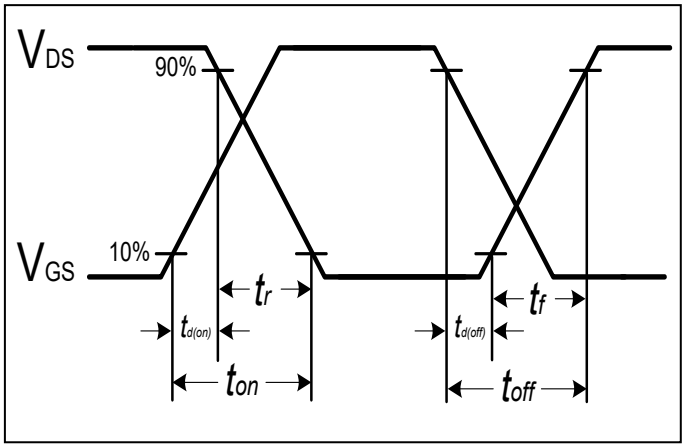


Fig. 2. Switching Time Waveform

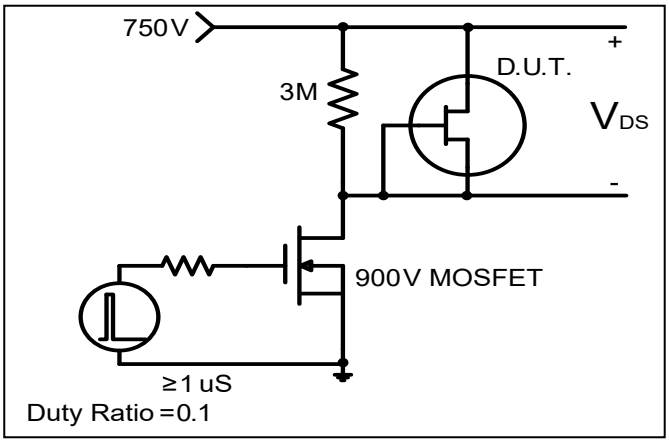


Fig. 3. Spike Voltage Test Circuit

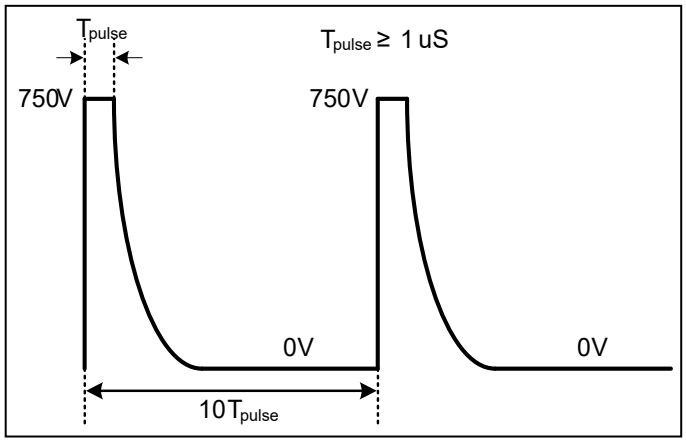


Fig. 4. Spike Voltage Waveform

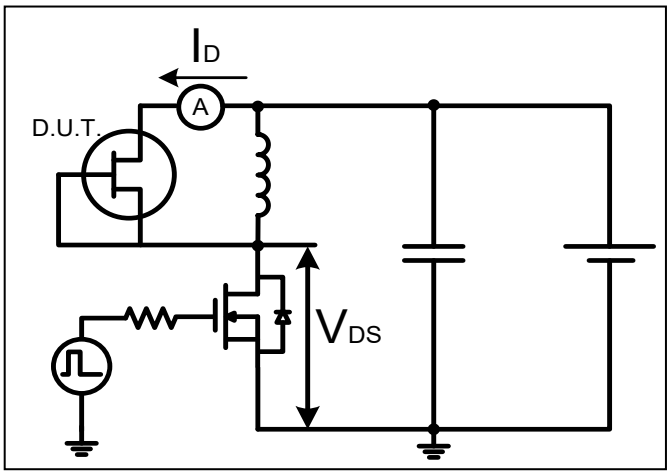


Fig. 5. Test Circuit for Diode Characteristics

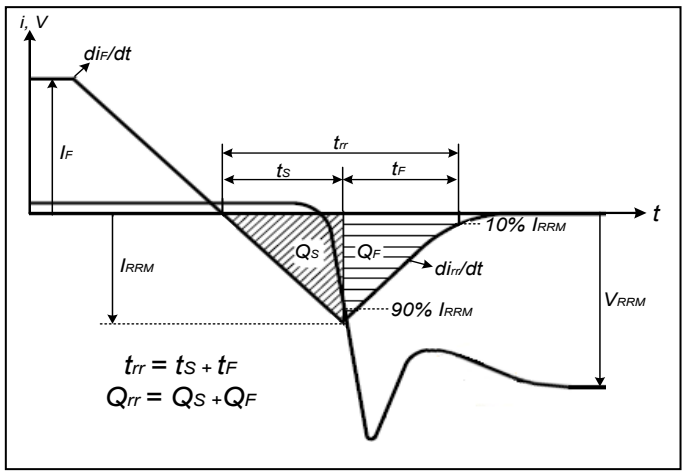
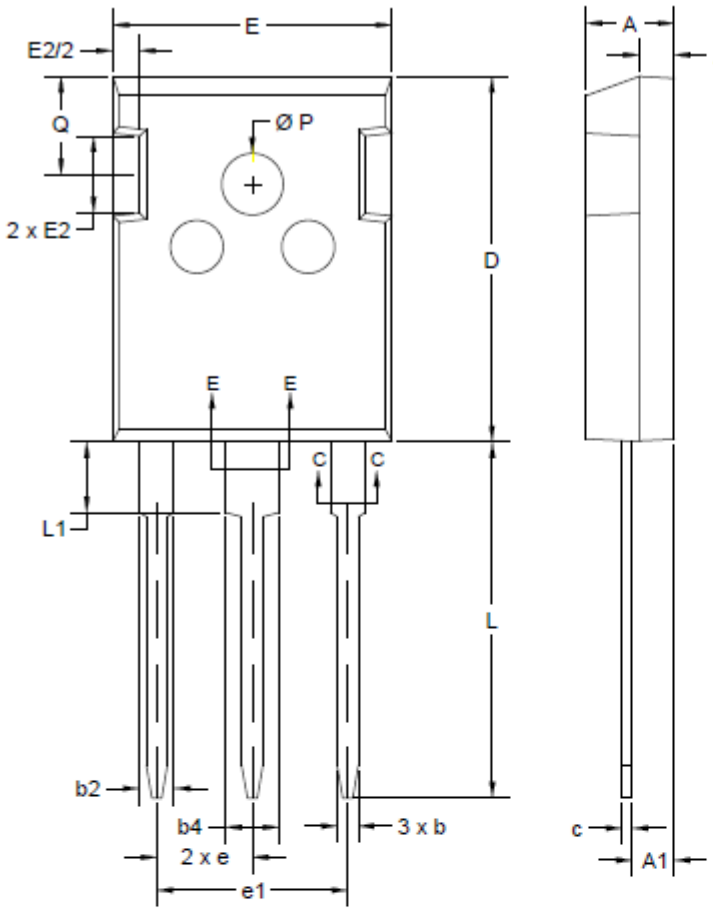
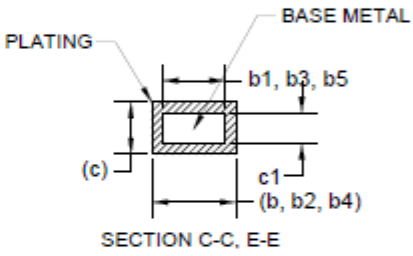


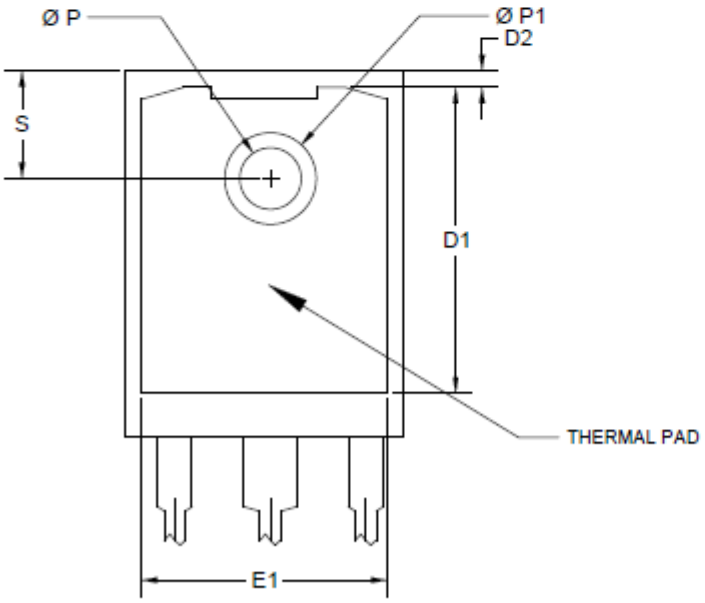
Fig. 6. Diode Recovery Waveform



SYMBOL	MILLIMETERS			INCHES		
	MINIMUM	NOMINAL	MAXIMUM	MINIMUM	NOMINAL	MAXIMUM
A	4.69	5.00	5.31	0.185	0.197	0.209
A1	2.20	2.39	2.59	0.087	0.094	0.102
A2	1.49	2.01	2.49	0.059	0.079	0.098
b	0.99	-	1.40	0.039	-	0.055
b1	0.99	-	1.35	0.039	-	0.053
b2	1.77	-	2.19	0.070	-	0.086
b3	1.77	-	2.14	0.070	-	0.084
b4	2.76	-	3.33	0.109	-	0.131
b5	2.76	-	3.28	0.109	-	0.129
c	0.38	-	0.89	0.015	-	0.035
c1	0.38	-	0.84	0.015	-	0.033
D	20.52	20.85	21.18	0.808	0.821	0.834
D1	16.51	-	-	0.650	-	-
D2	0.50	-	1.42	0.020	-	0.056
E	15.49	15.88	16.26	0.610	0.625	0.640
E1	13.46	-	-	0.530	-	-
E2	2.03	-	3.56	0.080	-	0.140
e	5.46 BSC			0.215 BSC		
e1	10.87 BSC			0.428 BSC		
L	20.01	20.27	20.52	0.788	0.798	0.808
L1	-	4.27	4.50	-	0.168	0.177
ØP	3.45	3.51	3.56	0.136	0.138	0.140
ØP1	-	-	7.39	-	-	0.291
Q	5.20	5.59	5.97	0.205	0.220	0.235
S	6.15 BSC			0.242 BSC		



SECTION C-C, E-E



NOTES:

1. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 MM (0.005") PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
2. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS D1 & E1.
3. LEAD FINISH UNCONTROLLED IN L1.
4. OUTLINE CONFORMS TO JEDEC TO-247AD.

TO-247 3L			
transphorm			
SCALE: 1:1	SHEET 1/1	DRAWING NO. 200019	VER. 2

Important Notice

Transphorm Gallium Nitride (GaN) Switches provide significant advantages over silicon (Si) Superjunction MOSFETs with lower gate charge, faster switching speeds and smaller reverse recovery charge. GaN Switches exhibit in-circuit switching speeds in excess of 150 V/ns and can be even pushed up to 500V/ns, compared to current silicon technology usually switching at rates less than 50V/ns.

The fast switching of GaN devices reduces current-voltage cross-over losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN Switches requires adherence to specific PCB layout guidelines and probing techniques .

Transphorm suggests visiting application note “Printed Circuit Board Layout and Probing for GaN Power Switches” before evaluating Transphorm GaN switches. Below are some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Switches	
DO	**DO NOT**
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing. Attach the probe and its ground connection directly to the test points	Use differential mode probe, or probe ground clip with long wire