FUJITSU SEMICONDUCTOR
DATA SHEET

DS702–00015–2v0-E

*8-bit Microcontrollers*

# New 8FX MB95810K Series

## MB95F814K/F816K/F818K

### ■ DESCRIPTION

The MB95810K Series is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of these series contain a variety of peripheral resources.

### ■ FEATURES

- F²MC-8FX CPU core
  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Bit test branch instructions
  - Bit manipulation instructions, etc.

Note: F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

- Clock
  - Selectable main clock source
    - Main oscillation clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)
    - External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
    - Main CR clock (4 MHz ±2%)
    - Main CR PLL clock
      - The main CR PLL clock frequency becomes 8 MHz ±2% when the PLL multiplication rate is 2.
      - The main CR PLL clock frequency becomes 10 MHz ±2% when the PLL multiplication rate is 2.5.
      - The main CR PLL clock frequency becomes 12 MHz ±2% when the PLL multiplication rate is 3.
      - The main CR PLL clock frequency becomes 16 MHz ±2% when the PLL multiplication rate is 4.
  - Selectable subclock source
    - Suboscillation clock (32.768 kHz)
    - External clock (32.768 kHz)
    - Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 150 kHz)
- Timer
  - 8/16-bit composite timer × 2 channels
  - 8/16-bit PPG × 2 channels
  - 16-bit PPG timer × 2 channels
  - 16-bit reload timer × 1 channel
  - Time-base timer × 1 channel
  - Watch prescaler × 1 channel

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FUJITSU SEMICONDUCTOR provides information facilitating product development via the following website. The website contains information useful for customers.

http://edevice.fujitsu.com/micom/en-support/


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- UART/SIO × 1 channel
  - Full duplex double buffer
  - Capable of clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer
- $I^2C$ bus interface × 1 channel
  Built-in wake-up function
- LIN-UART
  - Full duplex double buffer
  - Capable of clock asynchronous serial data transfer and clock synchronous serial data transfer
- External interrupt × 12 channels
  - Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
  - Can be used to wake up the device from different low power consumption (standby) modes
- 8/10-bit A/D converter × 12 channels
  8-bit or 10-bit resolution can be selected.
- Low power consumption (standby) modes
  There are four standby modes as follows:
  - Stop mode
  - Sleep mode
  - Watch mode
  - Time-base timer mode

  In standby mode, two further options can be selected: normal standby mode and deep standby mode.
- I/O port (no. of I/O ports: 58)
  - General-purpose I/O ports (CMOS I/O) : 54
  - General-purpose I/O ports (N-ch open drain) : 4
- On-chip debug
  - 1-wire serial control
  - Serial writing supported (asynchronous mode)
- Hardware/software watchdog timer
  - Built-in hardware watchdog timer
  - Built-in software watchdog timer
- Power-on reset
  A power-on reset is generated when the power is switched on.
- Low-voltage detection (LVD) reset circuit
  - The LVD function is enabled by default. For details, see “2. Recommended Operating Conditions” in “■ ELECTRICAL CHARACTERISTICS”.
  - The LVD function can be controlled through software.
  - The LVD reset circuit control register (LVDCC) enables or disables the LVD reset.
  - The LVD reset circuit has an internal low-voltage detector. The combination of detection voltage and release voltage can be selected from four options.
- Comparator × 2 channels
  - Built-in dedicated BGR
  - The comparator reference voltage can be selected between the BGR voltage and the comparator pin.
- Clock supervisor counter
  Built-in clock supervisor counter
- Dual operation Flash memory
  The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.
- Flash memory security function
  Protects the content of the Flash memory.

## ■ PRODUCT LINE-UP

| Part number / Parameter | MB95F814K | MB95F816K | MB95F818K |
|---|---|---|---|
| Type | Flash memory product | | |
| Clock supervisor counter | It supervises the main clock oscillation and the subclock oscillation. | | |
| Flash memory capacity | 20 Kbyte | 36 Kbyte | 60 Kbyte |
| RAM capacity | 512 bytes | 1 Kbyte | 2 Kbyte |
| Power-on reset | Yes | | |
| Low-voltage detection reset | Controlled through software | | |
| Reset input | Selected through software | | |
| CPU functions | • Number of basic instructions : 136<br>• Instruction bit length : 8 bits<br>• Instruction length : 1 to 3 bytes<br>• Data bit length : 1, 8 and 16 bits<br>• Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz)<br>• Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz) | | |
| General-purpose I/O | • I/O port : 58<br>• CMOS I/O : 54<br>• N-ch open drain : 4 | | |
| Time-base timer | Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz) | | |
| Hardware/ software watchdog timer | • Reset generation cycle<br>Main oscillation clock at 10 MHz: 105 ms (Min)<br>• The sub-CR clock can be used as the source clock of the software watchdog timer. | | |
| Wild register | It can be used to replace 3 bytes of data. | | |
| LIN-UART | • A wide range of communication speed can be selected by a dedicated reload timer.<br>• It has a full duplex double buffer.<br>• Both clock synchronous serial data transfer and clock asynchronous serial data transfer are enabled.<br>• The LIN function can be used as a LIN master or a LIN slave. | | |
| 8/10-bit A/D converter | 12 channels | | |
| | 8-bit or 10-bit resolution can be selected. | | |
| 8/16-bit composite timer | 2 channels | | |
| | • The timer can be configured as an “8-bit timer × 2 channels” or a “16-bit timer × 1 channel”.<br>• It has the following functions: interval timer function, PWC function, PWM function and input capture function.<br>• Count clock: it can be selected from internal clocks (seven types) and external clocks.<br>• It can output square wave. | | |
| External interrupt | 12 channels | | |
| | • Interrupt by edge detection (The rising edge, falling edge, and both edges can be selected.)<br>• It can be used to wake up the device from different standby modes. | | |
| On-chip debug | • 1-wire serial control<br>• It supports serial writing (asynchronous mode). | | |

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<table>
<tr><th>Part number<br>Parameter</th><th>MB95F814K</th><th>MB95F816K</th><th>MB95F818K</th></tr>
<tr><td rowspan="2">UART/SIO</td><td colspan="3">1 channel</td></tr>
<tr><td colspan="3">• Data transfer with UART/SIO is enabled.<br>• It has a full duplex double buffer, variable data length (5/6/7/8 bits), an internal baud rate generator and an error detection function.<br>• It uses the NRZ type transfer format.<br>• LSB-first data transfer and MSB-first data transfer are available to use.<br>• Both clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer are enabled.</td></tr>
<tr><td rowspan="2">I²C bus interface</td><td colspan="3">1 channel</td></tr>
<tr><td colspan="3">• Master/slave transmission and receiving<br>• It has the following functions: bus error function, arbitration function, transmission direction detection function, wake-up function, and functions of generating and detecting repeated START conditions.</td></tr>
<tr><td rowspan="2">8/16-bit PPG</td><td colspan="3">2 channels</td></tr>
<tr><td colspan="3">• Each channel can be used as an “8-bit timer × 2 channels” or a “16-bit timer × 1 channel”.<br>• The counter operating clock can be selected from eight clock sources.</td></tr>
<tr><td rowspan="2">16-bit PPG timer</td><td colspan="3">2 channels</td></tr>
<tr><td colspan="3">• PWM mode and one-shot mode are available to use.<br>• The counter operating clock can be selected from eight clock sources.<br>• It supports external trigger start.</td></tr>
<tr><td rowspan="2">16-bit reload timer</td><td colspan="3">1 channel</td></tr>
<tr><td colspan="3">• Two clock modes and two counter operating modes are available to use.<br>• It can output square wave.<br>• Count clock: it can be selected from internal clocks (seven types) and external clocks.<br>• Two counter operating modes: reload mode and one-shot mode</td></tr>
<tr><td>Watch counter</td><td colspan="3">• Count clock: it can be selected from eight clock sources from the watch prescaler.<br>• The counter value can be selected from 0 to 63. (The watch counter can count for one minute when the clock source of one second is selected and 60 is selected as the counter value.)</td></tr>
<tr><td>Watch prescaler</td><td colspan="3">Eight different time intervals can be selected.</td></tr>
<tr><td rowspan="2">Comparator</td><td colspan="3">2 channels</td></tr>
<tr><td colspan="3">The reference voltage of each channel can be selected between the BGR voltage and the comparator pin.</td></tr>
<tr><td>Flash memory</td><td colspan="3">• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands.<br>• It has a flag indicating the completion of the operation of Embedded Algorithm.<br>• Flash security feature for protecting the content of the Flash memory<br><table><tr><td>Number of program/erase cycles</td><td>1000</td><td>10000</td><td>100000</td></tr><tr><td>Data retention time</td><td>20 years</td><td>10 years</td><td>5 years</td></tr></table></td></tr>
<tr><td>Standby mode</td><td colspan="3">There are four standby modes as follows:<br>• Stop mode<br>• Sleep mode<br>• Watch mode<br>• Time-base timer mode<br>In standby mode, two further options can be selected: normal standby mode and deep standby mode</td></tr>
<tr><td>Package</td><td colspan="3">FPT-64P-M38<br>FPT-64P-M39</td></tr>
</table>

## ■ PACKAGES AND CORRESPONDING PRODUCTS

| Part number / Package | MB95F814K | MB95F816K | MB95F818K |
|---|---|---|---|
| FPT-64P-M38 | O | O | O |
| FPT-64P-M39 | O | O | O |

O: Available

## ■ DIFFERENCES AMONG PRODUCTS AND NOTES ON PRODUCT SELECTION

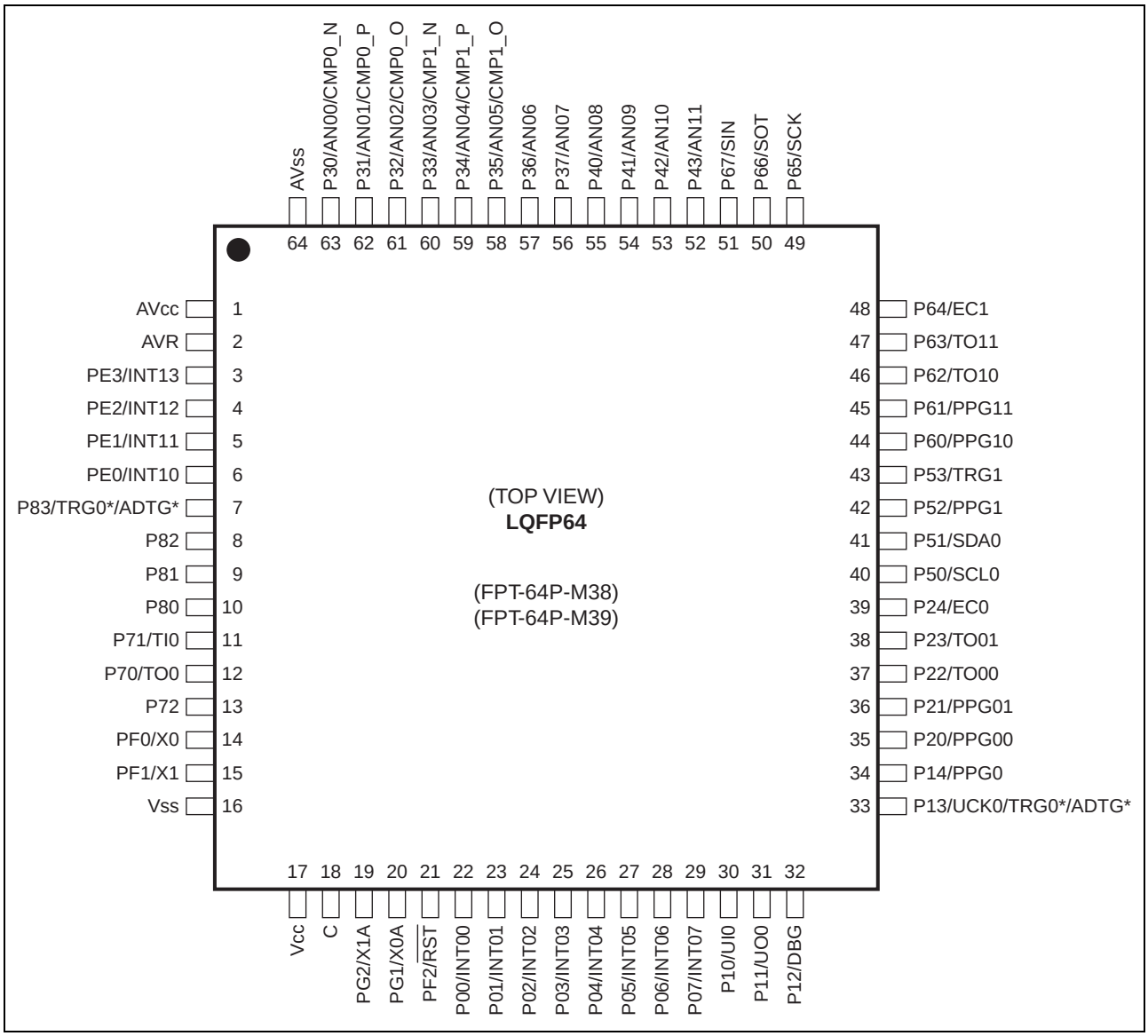
- Current consumption
  When using the on-chip debug function, take account of the current consumption of Flash program/erase.
  For details of current consumption, see “■ ELECTRICAL CHARACTERISTICS”.

- Package
  For details of information on each package, see “■ PACKAGES AND CORRESPONDING PRODUCTS” and “■ PACKAGE DIMENSION”.

- Operating voltage
  The operating voltage varies, depending on whether the on-chip debug function is used or not.
  For details of operating voltage, see “■ ELECTRICAL CHARACTERISTICS”.

- On-chip debug function
  The on-chip debug function requires that $V_{CC}$, $V_{SS}$ and one serial wire be connected to an evaluation tool.
  For details of the connection method, refer to “CHAPTER 25 EXAMPLE OF SERIAL PROGRAMMING CONNECTION” in “New 8FX MB95810K Series Hardware Manual”.

## ■ PIN ASSIGNMENT




*: TRG0 and ADTG can be mapped to either P13 or P83 by using the SYSC register.

## ■ PIN FUNCTIONS

| Pin no. | Pin name | I/O circuit type*1 | Function | I/O type | | | |
|---|---|---|---|---|---|---|---|
| | | | | Input | Output | OD*2 | PU*3 |
| 1 | AVCC | — | Analog power supply pin for 8/10-bit A/D converter | — | — | — | — |
| 2 | AVR | — | Reference input pin for 8/10-bit A/D converter | — | — | — | — |
| 3 | PE3 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | INT13 | | External interrupt input pin | | | | |
| 4 | PE2 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | INT12 | | External interrupt input pin | | | | |
| 5 | PE1 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | INT11 | | External interrupt input pin | | | | |
| 6 | PE0 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | INT10 | | External interrupt input pin | | | | |
| 7 | P83 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | TRG0*4 | | 16-bit PPG timer ch. 0 trigger input pin | | | | |
| | ADTG*4 | | 8/10-bit A/D converter trigger input pin | | | | |
| 8 | P82 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| 9 | P81 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| 10 | P80 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| 11 | P71 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | TI0 | | 16-bit reload timer ch. 0 input pin | | | | |
| 12 | P70 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | TO0 | | 16-bit reload timer ch. 0 output pin | | | | |
| 13 | P72 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| 14 | PF0 | B | General-purpose I/O port | Hysteresis | CMOS | — | — |
| | X0 | | Main clock input oscillation pin | | | | |
| 15 | PF1 | B | General-purpose I/O port | Hysteresis | CMOS | — | — |
| | X1 | | Main clock I/O oscillation pin | | | | |
| 16 | VSS | — | Power supply pin (GND) | — | — | — | — |
| 17 | VCC | — | Power supply pin | — | — | — | — |
| 18 | C | — | Decoupling capacitor connection pin | — | — | — | — |
| 19 | PG2 | C | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | X1A | | Subclock I/O oscillation pin | | | | |
| 20 | PG1 | C | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | X0A | | Subclock input oscillation pin | | | | |
| 21 | PF2 | A | General-purpose I/O port | Hysteresis | CMOS | O | — |
| | $\overline{RST}$ | | Reset pin | | | | |
| 22 | P00 | D | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | INT00 | | External interrupt input pin | | | | |
| 23 | P01 | D | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | INT01 | | External interrupt input pin | | | | |

*(Continued)*

| Pin no. | Pin name | I/O circuit type*1 | Function | I/O type | | | |
|---|---|---|---|---|---|---|---|
| | | | | Input | Output | OD*2 | PU*3 |
| 24 | P02 | D | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | INT02 | | External interrupt input pin | | | | |
| 25 | P03 | D | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | INT03 | | External interrupt input pin | | | | |
| 26 | P04 | D | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | INT04 | | External interrupt input pin | | | | |
| 27 | P05 | D | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | INT05 | | External interrupt input pin | | | | |
| 28 | P06 | D | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | INT06 | | External interrupt input pin | | | | |
| 29 | P07 | D | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | INT07 | | External interrupt input pin | | | | |
| 30 | P10 | I | General-purpose I/O port | CMOS | CMOS | — | O |
| | UI0 | | UART/SIO ch. 0 data input pin | | | | |
| 31 | P11 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | UO0 | | UART/SIO ch. 0 data output pin | | | | |
| 32 | P12 | G | General-purpose I/O port | Hysteresis | CMOS | O | — |
| | DBG | | DBG input pin | | | | |
| 33 | P13 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | UCK0 | | UART/SIO ch. 0 clock I/O pin | | | | |
| | TRG0*4 | | 16-bit PPG timer ch. 0 trigger input pin | | | | |
| | ADTG*4 | | 8/10-bit A/D converter trigger input pin | | | | |
| 34 | P14 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | PPG0 | | 16-bit PPG timer ch. 0 output pin | | | | |
| 35 | P20 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | PPG00 | | 8/16-bit PPG ch. 0 output pin | | | | |
| 36 | P21 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | PPG01 | | 8/16-bit PPG ch. 0 output pin | | | | |
| 37 | P22 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | TO00 | | 8/16-bit composite timer ch. 0 output pin | | | | |
| 38 | P23 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | TO01 | | 8/16-bit composite timer ch. 0 output pin | | | | |
| 39 | P24 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin | | | | |
| 40 | P50 | H | General-purpose I/O port | CMOS | CMOS | O | — |
| | SCL | | $I^2C$ bus interface ch. 0 clock I/O pin | | | | |
| 41 | P51 | H | General-purpose I/O port | CMOS | CMOS | O | — |
| | SDA | | $I^2C$ bus interface ch. 0 data I/O pin | | | | |

*(Continued)*

| Pin no. | Pin name | I/O circuit type*1 | Function | I/O type | | | |
|---|---|---|---|---|---|---|---|
| | | | | Input | Output | OD*2 | PU*3 |
| 42 | P52 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | PPG1 | | 16-bit PPG timer ch. 1 output pin | | | | |
| 43 | P53 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | TRG1 | | 16-bit PPG timer ch. 1 trigger input pin | | | | |
| 44 | P60 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | PPG10 | | 8/16-bit PPG ch. 1 output pin | | | | |
| 45 | P61 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | PPG11 | | 8/16-bit PPG ch. 1 output pin | | | | |
| 46 | P62 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | TO10 | | 8/16-bit composite timer ch. 1 output pin | | | | |
| 47 | P63 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | TO11 | | 8/16-bit composite timer ch. 1 output pin | | | | |
| 48 | P64 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | EC1 | | 8/16-bit composite timer ch. 1 clock input pin | | | | |
| 49 | P65 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | SCK | | LIN-UART clock I/O pin | | | | |
| 50 | P66 | F | General-purpose I/O port | Hysteresis | CMOS | — | O |
| | SOT | | LIN-UART data output pin | | | | |
| 51 | P67 | I | General-purpose I/O port | CMOS | CMOS | — | O |
| | SIN | | LIN-UART data input pin | | | | |
| 52 | P43 | E | General-purpose I/O port | Hysteresis/ analog | CMOS | — | O |
| | AN11 | | 8/10-bit A/D converter analog input pin | | | | |
| 53 | P42 | E | General-purpose I/O port | Hysteresis/ analog | CMOS | — | O |
| | AN10 | | 8/10-bit A/D converter analog input pin | | | | |
| 54 | P41 | E | General-purpose I/O port | Hysteresis/ analog | CMOS | — | O |
| | AN09 | | 8/10-bit A/D converter analog input pin | | | | |
| 55 | P40 | E | General-purpose I/O port | Hysteresis/ analog | CMOS | — | O |
| | AN08 | | 8/10-bit A/D converter analog input pin | | | | |
| 56 | P37 | E | General-purpose I/O port | Hysteresis/ analog | CMOS | — | O |
| | AN07 | | 8/10-bit A/D converter analog input pin | | | | |
| 57 | P36 | E | General-purpose I/O port | Hysteresis/ analog | CMOS | — | O |
| | AN06 | | 8/10-bit A/D converter analog input pin | | | | |
| 58 | P35 | E | General-purpose I/O port | Hysteresis/ analog | CMOS | — | O |
| | AN05 | | 8/10-bit A/D converter analog input pin | | | | |
| | CMP1_O | | Comparator ch. 1 digital output pin | | | | |
| 59 | P34 | E | General-purpose I/O port | Hysteresis/ analog | CMOS | — | O |
| | AN04 | | 8/10-bit A/D converter analog input pin | | | | |
| | CMP1_P | | Comparator ch. 1 non-inverting analog input (positive input) pin | | | | |

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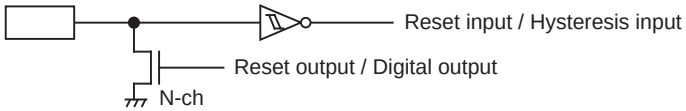
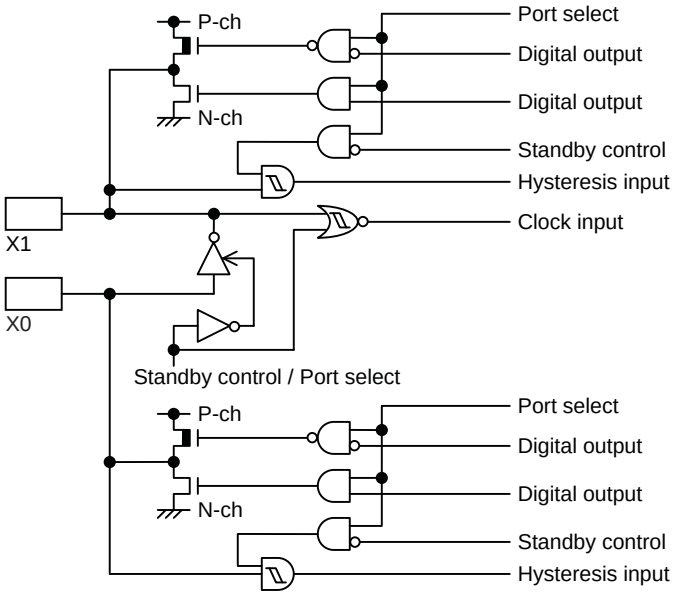
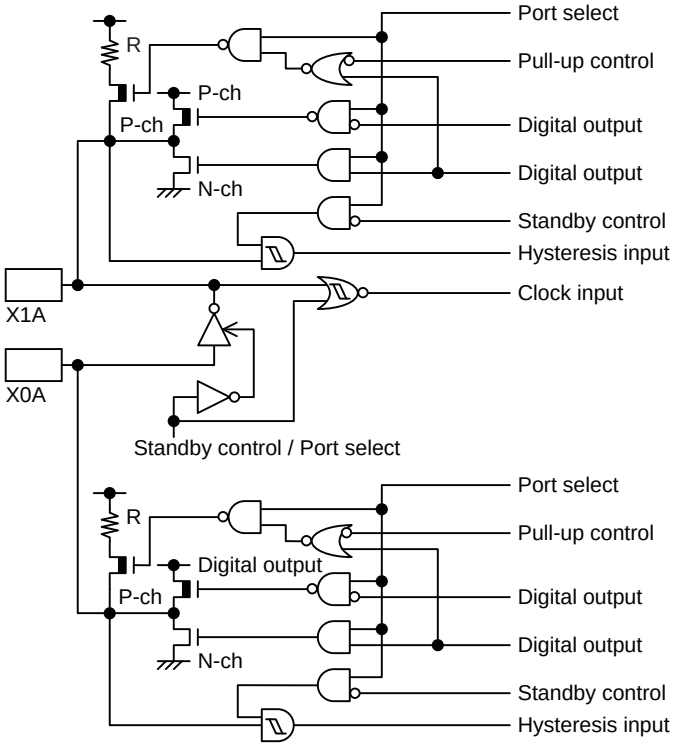
| Pin no. | Pin name | I/O circuit type*1 | Function | I/O type | | | |
|---|---|---|---|---|---|---|---|
| | | | | Input | Output | OD*2 | PU*3 |
| 60 | P33 | E | General-purpose I/O port | Hysteresis/ analog | CMOS | — | O |
| | AN03 | | 8/10-bit A/D converter analog input pin | | | | |
| | CMP1_N | | Comparator ch. 1 inverting analog input (negative input) pin | | | | |
| 61 | P32 | E | General-purpose I/O port | Hysteresis/ analog | CMOS | — | O |
| | AN02 | | 8/10-bit A/D converter analog input pin | | | | |
| | CMP0_O | | Comparator ch. 0 digital output pin | | | | |
| 62 | P31 | E | General-purpose I/O port | Hysteresis/ analog | CMOS | — | O |
| | AN01 | | 8/10-bit A/D converter analog input pin | | | | |
| | CMP0_P | | Comparator ch. 0 non-inverting analog input (positive input) pin | | | | |
| 63 | P30 | E | General-purpose I/O port | Hysteresis/ analog | CMOS | — | O |
| | AN00 | | 8/10-bit A/D converter analog input pin | | | | |
| | CMP0_N | | Comparator ch. 0 inverting analog input (negative input) pin | | | | |
| 64 | $AV_{SS}$ | — | 8/10-bit A/D converter power supply pin (GND) | — | — | — | — |

(O: Available)

*1: For the I/O circuit types, see “■ I/O CIRCUIT TYPE”.
*2: N-ch open drain
*3: Pull-up
*4: TRG0 and ADTG can be mapped to either P13 or P83 by using the SYSC register.

## ■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|---|---|---|
| A |  | • N-ch open drain output<br>• Hysteresis input<br>• Reset output |
| B |  | • Oscillation circuit<br>• High-speed side Feedback resistance: approx. 1 MΩ<br>• CMOS output<br>• Hysteresis input |
| C |  | • Oscillation circuit<br>• Low-speed side Feedback resistance: approx. 5 MΩ<br>• CMOS output<br>• Hysteresis input<br>• Pull-up control |

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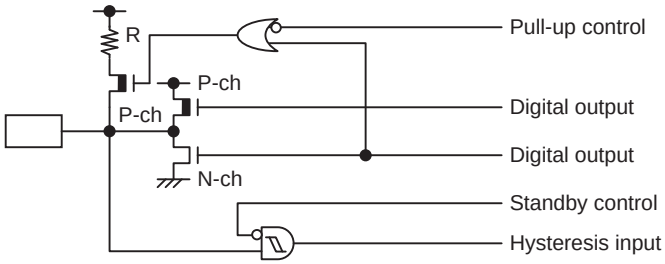
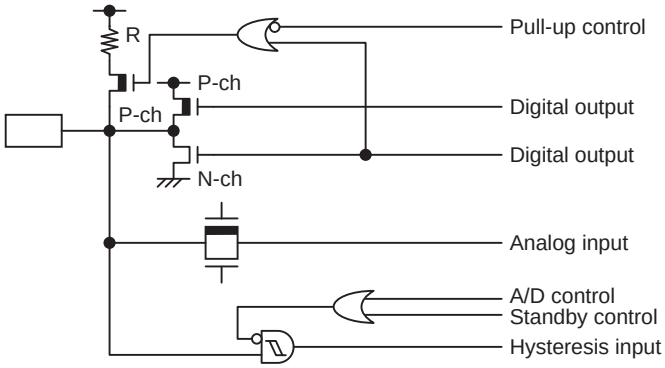
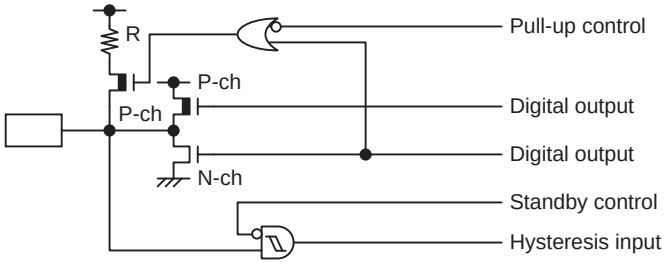
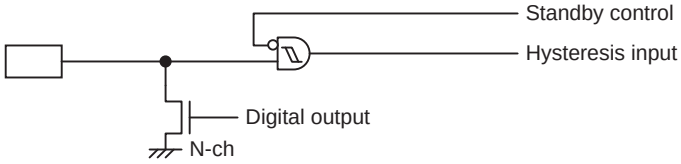
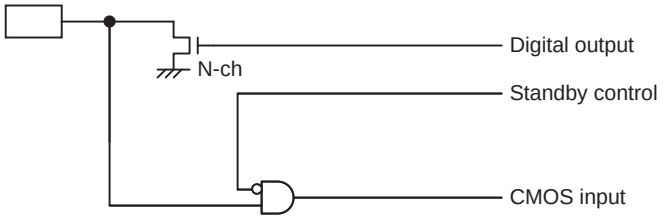
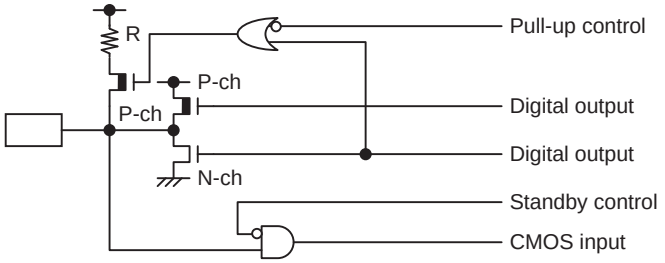
*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| D |  | • CMOS output<br>• Hysteresis input<br>• Pull-up control<br>• High current output |
| E |  | • CMOS output<br>• Hysteresis input<br>• Pull-up control<br>• Analog input |
| F |  | • CMOS output<br>• Hysteresis input<br>• Pull-up control |
| G |  | • N-ch open drain output<br>• Hysteresis input |
| H |  | • N-ch open drain output<br>• CMOS input |
| I |  | • CMOS output<br>• CMOS input<br>• Pull-up control |

## ■ HANDLING PRECAUTIONS

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your FUJITSU SEMICONDUCTOR semiconductor devices.

### 1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

- **Absolute Maximum Ratings**

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

- **Recommended Operating Conditions**

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

- **Processing and Protection of Pins**

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- **Latch-up**

  Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

  CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

  (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

  (2) Be sure that abnormal current flows do not occur during the power-on sequence.

- **Observance of Safety Regulations and Standards**

  Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- **Fail-Safe Design**

  Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- **Precautions Related to Usage of Devices**

  FUJITSU SEMICONDUCTOR semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

  CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

## 2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under FUJITSU SEMICONDUCTOR's recommended conditions. For detailed information about mount conditions, contact your sales representative.

- **Lead Insertion Type**

  Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

  Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to FUJITSU SEMICONDUCTOR recommended mounting conditions.

  If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

- **Surface Mount Type**

  Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

  You must use appropriate mounting techniques. FUJITSU SEMICONDUCTOR recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with FUJITSU SEMICONDUCTOR ranking of recommended conditions.

- **Lead-Free Packaging**

  CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- **Storage of Semiconductor Devices**

  Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

  (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

  (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5 °C and 30 °C.
  When you open Dry Package that recommends humidity 40% to 70% relative humidity.

  (3) When necessary, FUJITSU SEMICONDUCTOR packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

  (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- **Baking**

  Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the FUJITSU SEMICONDUCTOR recommended conditions for baking.

  Condition: 125 °C/24 h

- **Static Electricity**

  Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

  (1) Maintain relative humidity in the working environment between 40% and 70%.
  Use of an apparatus for ion generation may be needed to remove electricity.

  (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

  (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
  Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

  (4) Ground all fixtures and instruments, or protect with anti-static measures.

  (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

## 3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of FUJITSU SEMICONDUCTOR products in other special environmental conditions should consult with sales representatives.

Please check the latest handling precautions at the following URL.
http://edevice.fujitsu.com/fj/handling-e.pdf

## ■ NOTES ON DEVICE HANDLING

- Preventing latch-ups

  When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.
  In a CMOS IC, if a voltage higher than $V_{CC}$ or a voltage lower than $V_{SS}$ is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in “1. Absolute Maximum Ratings” of “■ ELECTRICAL CHARACTERISTICS” is applied to the $V_{CC}$ pin or the $V_{SS}$ pin, a latch-up may occur.
  When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

- Stabilizing supply voltage

  Supply voltage must be stabilized.
  A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the $V_{CC}$ power supply voltage.
  As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in $V_{CC}$ ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard $V_{CC}$ value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

- Notes on using the external clock

  When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

## ■ PIN CONNECTION

- Treatment of unused pins

  If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

- Power supply pins

  To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the $V_{CC}$ pin and the $V_{SS}$ pin to the power supply and ground outside the device. In addition, connect the current supply source to the $V_{CC}$ pin and the $V_{SS}$ pin with low impedance.
  It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between the $V_{CC}$ pin and the $V_{SS}$ pin at a location close to this device.

- DBG pin

  Connect the DBG pin to an external pull-up resistor of 2 kΩ or above.
  After power-on, ensure that the DBG pin does not stay at “L” level until the reset output is released.
  The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

- $\overline{\text{RST}}$ pin

  Connect the $\overline{\text{RST}}$ pin to an external pull-up resistor of 2 kΩ or above.
  To prevent the device from unintentionally entering the reset mode due to noise, minimize the interconnection length between a pull-up resistor and the $\overline{\text{RST}}$ pin and that between a pull-up resistor and the $V_{CC}$ pin when designing the layout of the printed circuit board.
  The PF2/$\overline{\text{RST}}$ pin functions as the reset input/output pin after power-on. In addition, the reset output of the PF2/$\overline{\text{RST}}$ pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit in the SYSC register.

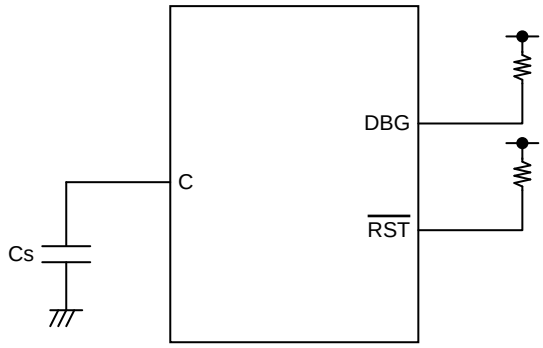
- Analog power supply

  Always set the same potential to the $AV_{CC}$ pin and the $V_{CC}$ pin. When $V_{CC}$ is larger than $AV_{CC}$, the current may flow through the AN00 to AN11 pins.

- Treatment of power supply pins on the 8/10-bit A/D converter
  Ensure that $AV_{CC}$ is equal to $V_{CC}$ and $AV_{SS}$ equal to $V_{SS}$ even when the 8/10-bit A/D converter is not in use. Noise riding on the $AV_{CC}$ pin may cause accuracy degradation. Therefore, connect a ceramic capacitor of 0.1 µF (approx.) as a bypass capacitor between the $AV_{CC}$ pin and the $AV_{SS}$ pin in the vicinity of this device.

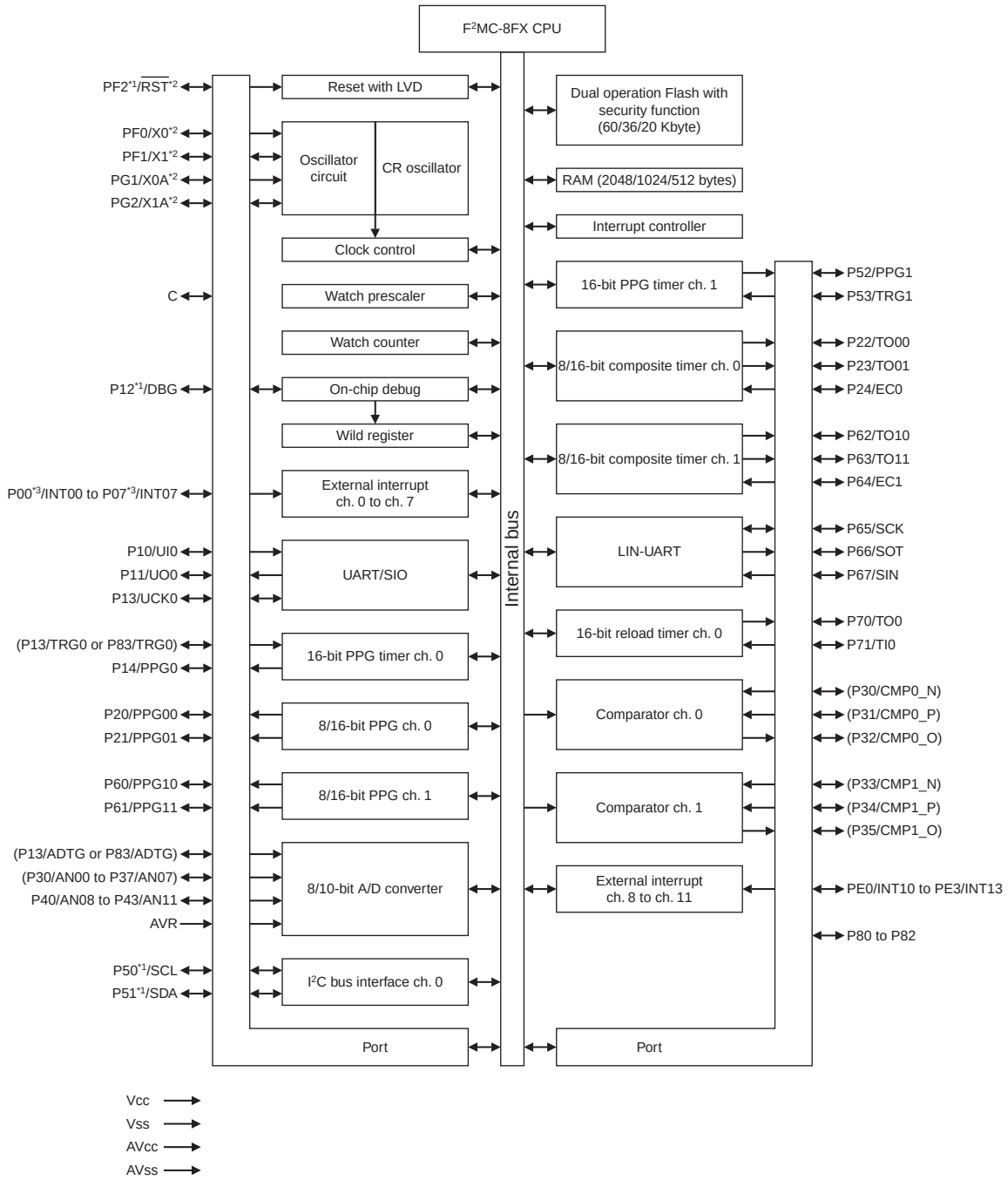
- C pin
  Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the $V_{CC}$ pin must have a capacitance equal to or larger than the capacitance of $C_S$. For the connection to a decoupling capacitor $C_S$, see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and $C_S$ and the distance between $C_S$ and the $V_{SS}$ pin when designing the layout of a printed circuit board.

- DBG/$\overline{\text{RST}}$/C pins connection diagram




- Note on serial communication
  In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed circuit board to prevent noise from occurring. Taking account of the reception of wrong data, take measures such as adding a checksum to the end of data in order to detect errors. If an error is detected, retransmit the data.

## ■ BLOCK DIAGRAM




*1: P12, P50, P51 and PF2 are N-ch open drain pins.

*2: Software select

*3: P00 to P07 are high-current pins.

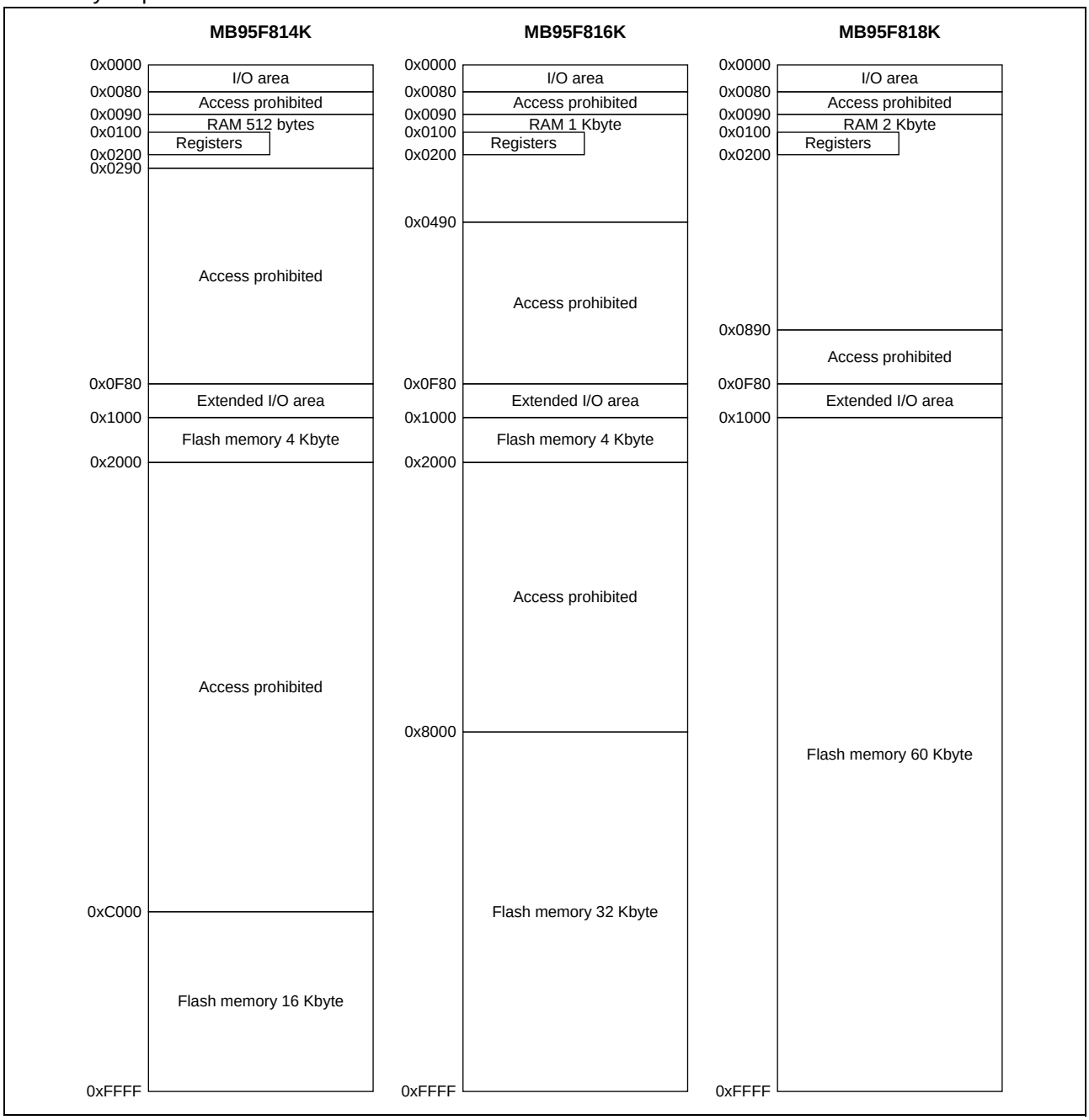
Note: Pins in parentheses indicate that those pins are shared among different peripheral functions.

## ■ CPU CORE

- Memory space

  The memory space of the MB95810K Series is 64 Kbyte in size, and consists of an I/O area, an extended I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95810K Series are shown below.

- Memory maps



## ■ MEMORY SPACE

The memory space of the MB95810K Series is 64 Kbyte in size, and consists of an I/O area, an extended I/O area, a data area, and a program area. The memory space includes areas for specific applications such as general-purpose registers and a vector table.

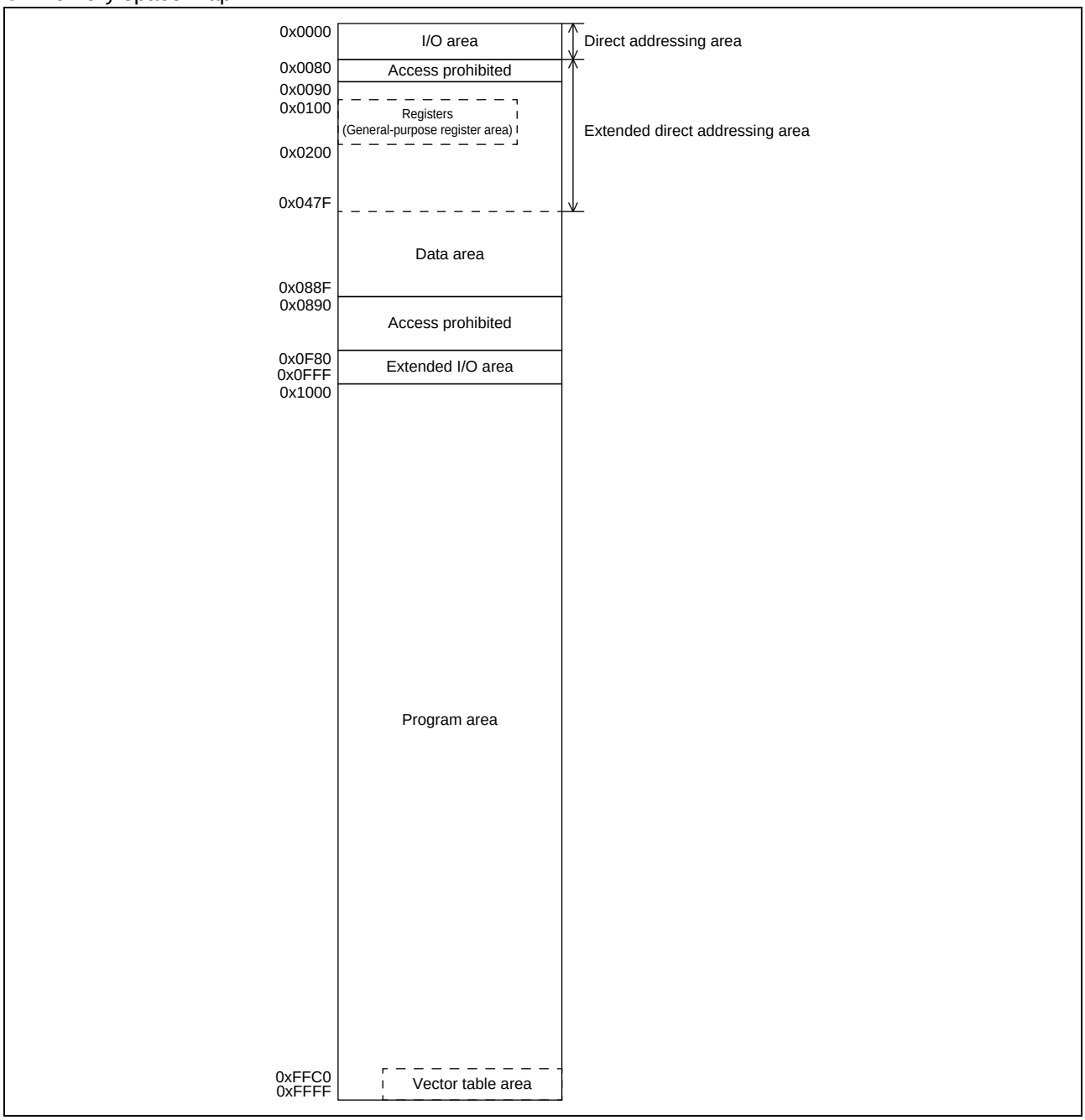
- I/O area (addresses: 0x0000 to 0x007F)
  - This area contains the control registers and data registers for built-in peripheral functions.
  - As the I/O area forms part of the memory space, it can be accessed in the same way as the memory. It can also be accessed at high-speed by using direct addressing instructions.

- Extended I/O area (addresses: 0x0F80 to 0x0FFF)
  - This area contains the control registers and data registers for built-in peripheral functions.
  - As the extended I/O area forms part of the memory space, it can be accessed in the same way as the memory.

- Data area
  - Static RAM is incorporated in the data area as the internal data area.
  - The internal RAM size varies according to product.
  - The RAM area from 0x0090 to 0x00FF can be accessed at high-speed by using direct addressing instructions.
  - In MB95F818K, the area from 0x0090 to 0x047F is an extended direct addressing area. It can be accessed at high-speed by direct addressing instructions with a direct bank pointer set.
  - In MB95F816K, the area from 0x0090 to 0x047F is an extended direct addressing area. It can be accessed at high-speed by direct addressing instructions with a direct bank pointer set.
  - In MB95F814K, the area from 0x0090 to 0x028F is an extended direct addressing area. It can be accessed at high-speed by direct addressing instructions with a direct bank pointer set.
  - The area from 0x0100 to 0x01FF can be used as a general-purpose register area.

- Program area
  - The Flash memory is incorporated in the program area as the internal program area.
  - The Flash memory size varies according to product.
  - The area from 0xFFC0 to 0xFFFF is used as the vector table.
  - The area from 0xFFBB to 0xFFBF is used to store data of the non-volatile register.

● Memory space map



## ■ AREAS FOR SPECIFIC APPLICATIONS

The general-purpose register area and vector table area are used for the specific applications.

- General-purpose register area (Addresses: 0x0100 to 0x01FF)
  - This area contains the auxiliary registers used for 8-bit arithmetic operations, transfer, etc.
  - As this area forms part of the RAM area, it can also be used as conventional RAM.
  - When the area is used as general-purpose registers, general-purpose register addressing enables high-speed access with short instructions.

- Non-volatile register data area (Addresses: 0xFFBB to 0xFFBF)
  - The area from 0xFFBB to 0xFFBF is used to store data of the non-volatile register. For details, refer to “CHAPTER 27 NON-VOLATILE REGISTER (NVR) INTERFACE” in “New 8FX MB95810K Series Hardware Manual”.

- Vector table area (Addresses: 0xFFC0 to 0xFFFF)
  - This area is used as the vector table for vector call instructions (CALLV), interrupts, and resets.
  - The top of the Flash memory area is allocated to the vector table area. The start address of a service routine is set to an address in the vector table in the form of data.

  “■ INTERRUPT SOURCE TABLE” lists the vector table addresses corresponding to vector call instructions, interrupts, and resets.
  For details, refer to “CHAPTER 4 RESET”, “CHAPTER 5 INTERRUPTS” and “A.2 Special Instruction ■ Special Instruction ● CALLV #vct” in “APPENDIX” in “New 8FX MB95810K Series Hardware Manual”.

- Direct bank pointer and access area

| Direct bank pointer (DP[2:0]) | Operand-specified dir | Access area |
|---|---|---|
| 0bXXX (It does not affect mapping.) | 0x0000 to 0x007F | 0x0000 to 0x007F |
| 0b000 (initial value) | 0x0090 to 0x00FF | 0x0090 to 0x00FF |
| 0b001 | 0x0080 to 0x00FF | 0x0100 to 0x017F |
| 0b010 | | 0x0180 to 0x01FF |
| 0b011 | | 0x0200 to 0x027F |
| 0b100 | | 0x0280 to 0x02FF*1 |
| 0b101 | | 0x0300 to 0x037F |
| 0b110 | | 0x0380 to 0x03FF |
| 0b111 | | 0x0400 to 0x047F*2 |

*1: Due to the memory size limit, the available access area is up to “0x028F” in MB95F814K.
*2: Due to the memory size limit, the available access area is up to “0x047F” in MB95F816K/F818K.

## ■ I/O MAP

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0x0000 | PDR0 | Port 0 data register | R/W | 0b00000000 |
| 0x0001 | DDR0 | Port 0 direction register | R/W | 0b00000000 |
| 0x0002 | PDR1 | Port 1 data register | R/W | 0b00000000 |
| 0x0003 | DDR1 | Port 1 direction register | R/W | 0b00000000 |
| 0x0004 | — | (Disabled) | — | — |
| 0x0005 | WATR | Oscillation stabilization wait time setting register | R/W | 0b11111111 |
| 0x0006 | PLLC | PLL control register | R/W | 0b000X0000 |
| 0x0007 | SYCC | System clock control register | R/W | 0bXXX11011 |
| 0x0008 | STBC | Standby control register | R/W | 0b00000000 |
| 0x0009 | RSRR | Reset source register | R/W | 0b000XXXXX |
| 0x000A | TBTC | Time-base timer control register | R/W | 0b00000000 |
| 0x000B | WPCR | Watch prescaler control register | R/W | 0b00000000 |
| 0x000C | WDTC | Watchdog timer control register | R/W | 0b00XX0000 |
| 0x000D | SYCC2 | System clock control register 2 | R/W | 0bXXXX0011 |
| 0x000E | PDR2 | Port 2 data register | R/W | 0b00000000 |
| 0x000F | DDR2 | Port 2 direction register | R/W | 0b00000000 |
| 0x0010 | PDR3 | Port 3 data register | R/W | 0b00000000 |
| 0x0011 | DDR3 | Port 3 direction register | R/W | 0b00000000 |
| 0x0012 | PDR4 | Port 4 data register | R/W | 0b00000000 |
| 0x0013 | DDR4 | Port 4 direction register | R/W | 0b00000000 |
| 0x0014 | PDR5 | Port 5 data register | R/W | 0b00000000 |
| 0x0015 | DDR5 | Port 5 direction register | R/W | 0b00000000 |
| 0x0016 | PDR6 | Port 6 data register | R/W | 0b00000000 |
| 0x0017 | DDR6 | Port 6 direction register | R/W | 0b00000000 |
| 0x0018 | PDR7 | Port 7 data register | R/W | 0b00000000 |
| 0x0019 | DDR7 | Port 7 direction register | R/W | 0b00000000 |
| 0x001A | PDR8 | Port 8 data register | R/W | 0b00000000 |
| 0x001B | DDR8 | Port 8 direction register | R/W | 0b00000000 |
| 0x001C | STBC2 | Standby control register 2 | R/W | 0b00000000 |
| 0x001D to 0x0024 | — | (Disabled) | — | — |
| 0x0025 | PUL8 | Port 8 pull-up register | R/W | 0b00000000 |
| 0x0026 | PDRE | Port E data register | R/W | 0b00000000 |
| 0x0027 | DDRE | Port E direction register | R/W | 0b00000000 |
| 0x0028 | PDRF | Port F data register | R/W | 0b00000000 |
| 0x0029 | DDRF | Port F direction register | R/W | 0b00000000 |
| 0x002A | PDRG | Port G data register | R/W | 0b00000000 |
| 0x002B | DDRG | Port G direction register | R/W | 0b00000000 |
| 0x002C | PUL0 | Port 0 pull-up register | R/W | 0b00000000 |

*(Continued)*

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0x002D | PUL1 | Port 1 pull-up register | R/W | 0b00000000 |
| 0x002E | PUL2 | Port 2 pull-up register | R/W | 0b00000000 |
| 0x002F | PUL3 | Port 3 pull-up register | R/W | 0b00000000 |
| 0x0030 | PUL4 | Port 4 pull-up register | R/W | 0b00000000 |
| 0x0031 | PUL5 | Port 5 pull-up register | R/W | 0b00000000 |
| 0x0032 | PUL7 | Port 7 pull-up register | R/W | 0b00000000 |
| 0x0033 | PUL6 | Port 6 pull-up register | R/W | 0b00000000 |
| 0x0034 | PULE | Port E pull-up register | R/W | 0b00000000 |
| 0x0035 | PULG | Port G pull-up register | R/W | 0b00000000 |
| 0x0036 | T01CR1 | 8/16-bit composite timer 01 status control register 1 | R/W | 0b00000000 |
| 0x0037 | T00CR1 | 8/16-bit composite timer 00 status control register 1 | R/W | 0b00000000 |
| 0x0038 | T11CR1 | 8/16-bit composite timer 11 status control register 1 | R/W | 0b00000000 |
| 0x0039 | T10CR1 | 8/16-bit composite timer 10 status control register 1 | R/W | 0b00000000 |
| 0x003A | PC01 | 8/16-bit PPG timer 01 control register | R/W | 0b00000000 |
| 0x003B | PC00 | 8/16-bit PPG timer 00 control register | R/W | 0b00000000 |
| 0x003C | PC11 | 8/16-bit PPG timer 11 control register | R/W | 0b00000000 |
| 0x003D | PC10 | 8/16-bit PPG timer 10 control register | R/W | 0b00000000 |
| 0x003E | TMCSRH0 | 16-bit reload timer control status register (upper) ch. 0 | R/W | 0b00000000 |
| 0x003F | TMCSRL0 | 16-bit reload timer control status register (lower) ch. 0 | R/W | 0b00000000 |
| 0x0040, 0x0041 | — | (Disabled) | — | — |
| 0x0042 | PCNTH0 | 16-bit PPG status control register (upper) ch. 0 | R/W | 0b00000000 |
| 0x0043 | PCNTL0 | 16-bit PPG status control register (lower) ch. 0 | R/W | 0b00000000 |
| 0x0044 | PCNTH1 | 16-bit PPG status control register (upper) ch. 1 | R/W | 0b00000000 |
| 0x0045 | PCNTL1 | 16-bit PPG status control register (lower) ch. 1 | R/W | 0b00000000 |
| 0x0046, 0x0047 | — | (Disabled) | — | — |
| 0x0048 | EIC00 | External interrupt circuit control register ch. 0/ch. 1 | R/W | 0b00000000 |
| 0x0049 | EIC10 | External interrupt circuit control register ch. 2/ch. 3 | R/W | 0b00000000 |
| 0x004A | EIC20 | External interrupt circuit control register ch. 4/ch. 5 | R/W | 0b00000000 |
| 0x004B | EIC30 | External interrupt circuit control register ch. 6/ch. 7 | R/W | 0b00000000 |
| 0x004C | EIC01 | External interrupt circuit control register ch. 10/ch. 11 | R/W | 0b00000000 |
| 0x004D | EIC11 | External interrupt circuit control register ch. 12/ch. 13 | R/W | 0b00000000 |
| 0x004E | LVDR | LVD reset voltage selection ID register | R/W | 0b00000000 |
| 0x004F | LVDCC | LVD reset circuit control register | R/W | 0b00000001 |
| 0x0050 | SCR | LIN-UART serial control register | R/W | 0b00000000 |
| 0x0051 | SMR | LIN-UART serial mode register | R/W | 0b00000000 |
| 0x0052 | SSR | LIN-UART serial status register | R/W | 0b00001000 |
| 0x0053 | RDR | LIN-UART receive data register | R/W | 0b00000000 |
| | TDR | LIN-UART transmit data register | | |

*(Continued)*

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0x0054 | ESCR | LIN-UART extended status control register | R/W | 0b00000100 |
| 0x0055 | ECCR | LIN-UART extended communication control register | R/W | 0b000000XX |
| 0x0056 | SMC10 | UART/SIO serial mode control register 1 ch. 0 | R/W | 0b00000000 |
| 0x0057 | SMC20 | UART/SIO serial mode control register 2 ch. 0 | R/W | 0b00100000 |
| 0x0058 | SSR0 | UART/SIO serial status and data register ch. 0 | R/W | 0b00000001 |
| 0x0059 | TDR0 | UART/SIO serial output data register ch. 0 | R/W | 0b00000000 |
| 0x005A | RDR0 | UART/SIO serial input data register ch. 0 | R | 0b00000000 |
| 0x005B | CMR0 | Comparator control register ch. 0 | R/W | 0b11000101 |
| 0x005C | CMR1 | Comparator control register ch. 1 | R/W | 0b11000101 |
| 0x005D to 0x005F | — | (Disabled) | — | — |
| 0x0060 | IBCR00 | $I^2C$ bus control register 0 ch. 0 | R/W | 0b00000000 |
| 0x0061 | IBCR10 | $I^2C$ bus control register 1 ch. 0 | R/W | 0b00000000 |
| 0x0062 | IBSR0 | $I^2C$ bus status register ch. 0 | R/W | 0b00000000 |
| 0x0063 | IDDR0 | $I^2C$ data register ch. 0 | R/W | 0b00000000 |
| 0x0064 | IAAR0 | $I^2C$ address register ch. 0 | R/W | 0b00000000 |
| 0x0065 | ICCR0 | $I^2C$ clock control register ch. 0 | R/W | 0b00000000 |
| 0x0066 to 0x006B | — | (Disabled) | — | — |
| 0x006C | ADC1 | 8/10-bit A/D converter control register 1 | R/W | 0b00000000 |
| 0x006D | ADC2 | 8/10-bit A/D converter control register 2 | R/W | 0b00000000 |
| 0x006E | ADDH | 8/10-bit A/D converter data register (upper) | R/W | 0b00000000 |
| 0x006F | ADDL | 8/10-bit A/D converter data register (lower) | R/W | 0b00000000 |
| 0x0070 | WCSR | Watch counter control register | R/W | 0b00000000 |
| 0x0071 | FSR2 | Flash memory status register 2 | R/W | 0b00000000 |
| 0x0072 | FSR | Flash memory status register | R/W | 0b000X0000 |
| 0x0073 | SWRE0 | Flash memory sector write control register 0 | R/W | 0b00000000 |
| 0x0074 | FSR3 | Flash memory status register 3 | R | 0b000XXXXX |
| 0x0075 | FSR4 | Flash memory status register 4 | R/W | 0b00000000 |
| 0x0076 | WREN | Wild register address compare enable register | R/W | 0b00000000 |
| 0x0077 | WROR | Wild register data test setting register | R/W | 0b00000000 |
| 0x0078 | — | Mirror of register bank pointer (RP) and direct bank pointer (DP) | — | — |
| 0x0079 | ILR0 | Interrupt level setting register 0 | R/W | 0b11111111 |
| 0x007A | ILR1 | Interrupt level setting register 1 | R/W | 0b11111111 |
| 0x007B | ILR2 | Interrupt level setting register 2 | R/W | 0b11111111 |
| 0x007C | ILR3 | Interrupt level setting register 3 | R/W | 0b11111111 |
| 0x007D | ILR4 | Interrupt level setting register 4 | R/W | 0b11111111 |
| 0x007E | ILR5 | Interrupt level setting register 5 | R/W | 0b11111111 |

*(Continued)*

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0x007F | — | (Disabled) | — | — |
| 0x0F80 | WRARH0 | Wild register address setting register (upper) ch. 0 | R/W | 0b00000000 |
| 0x0F81 | WRARL0 | Wild register address setting register (lower) ch. 0 | R/W | 0b00000000 |
| 0x0F82 | WRDR0 | Wild register data setting register ch. 0 | R/W | 0b00000000 |
| 0x0F83 | WRARH1 | Wild register address setting register (upper) ch. 1 | R/W | 0b00000000 |
| 0x0F84 | WRARL1 | Wild register address setting register (lower) ch. 1 | R/W | 0b00000000 |
| 0x0F85 | WRDR1 | Wild register data setting register ch. 1 | R/W | 0b00000000 |
| 0x0F86 | WRARH2 | Wild register address setting register (upper) ch. 2 | R/W | 0b00000000 |
| 0x0F87 | WRARL2 | Wild register address setting register (lower) ch. 2 | R/W | 0b00000000 |
| 0x0F88 | WRDR2 | Wild register data setting register ch. 2 | R/W | 0b00000000 |
| 0x0F89 to 0x0F91 | — | (Disabled) | — | — |
| 0x0F92 | T01CR0 | 8/16-bit composite timer 01 status control register 0 | R/W | 0b00000000 |
| 0x0F93 | T00CR0 | 8/16-bit composite timer 00 status control register 0 | R/W | 0b00000000 |
| 0x0F94 | T01DR | 8/16-bit composite timer 01 data register | R/W | 0b00000000 |
| 0x0F95 | T00DR | 8/16-bit composite timer 00 data register | R/W | 0b00000000 |
| 0x0F96 | TMCR0 | 8/16-bit composite timer 00/01 timer mode control register | R/W | 0b00000000 |
| 0x0F97 | T11CR0 | 8/16-bit composite timer 11 status control register 0 | R/W | 0b00000000 |
| 0x0F98 | T10CR0 | 8/16-bit composite timer 10 status control register 0 | R/W | 0b00000000 |
| 0x0F99 | T11DR | 8/16-bit composite timer 11 data register | R/W | 0b00000000 |
| 0x0F9A | T10DR | 8/16-bit composite timer 10 data register | R/W | 0b00000000 |
| 0x0F9B | TMCR1 | 8/16-bit composite timer 10/11 timer mode control register | R/W | 0b00000000 |
| 0x0F9C | PPS01 | 8/16-bit PPG01 cycle setting buffer register | R/W | 0b11111111 |
| 0x0F9D | PPS00 | 8/16-bit PPG00 cycle setting buffer register | R/W | 0b11111111 |
| 0x0F9E | PDS01 | 8/16-bit PPG01 duty setting buffer register | R/W | 0b11111111 |
| 0x0F9F | PDS00 | 8/16-bit PPG00 duty setting buffer register | R/W | 0b11111111 |
| 0x0FA0 | PPS11 | 8/16-bit PPG11 cycle setting buffer register | R/W | 0b11111111 |
| 0x0FA1 | PPS10 | 8/16-bit PPG10 cycle setting buffer register | R/W | 0b11111111 |
| 0x0FA2 | PDS11 | 8/16-bit PPG11 duty setting buffer register | R/W | 0b11111111 |
| 0x0FA3 | PDS10 | 8/16-bit PPG10 duty setting buffer register | R/W | 0b11111111 |
| 0x0FA4 | PPGS | 8/16-bit PPG start register | R/W | 0b00000000 |
| 0x0FA5 | REVC | 8/16-bit PPG output inversion register | R/W | 0b00000000 |
| 0x0FA6 | TMRH0 | 16-bit reload timer timer register (upper) ch. 0 | R/W | 0b00000000 |
| | TMRLRH0 | 16-bit reload timer reload register (upper) ch. 0 | | |
| 0x0FA7 | TMRL0 | 16-bit reload timer timer register (lower) ch. 0 | R/W | 0b00000000 |
| | TMRLRL0 | 16-bit reload timer reload register (lower) ch. 0 | | |
| 0x0FA8, 0x0FA9 | — | (Disabled) | — | — |

*(Continued)*

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0x0FAA | PDCRH0 | 16-bit PPG downcounter register (upper) ch. 0 | R | 0b00000000 |
| 0x0FAB | PDCRL0 | 16-bit PPG downcounter register (lower) ch. 0 | R | 0b00000000 |
| 0x0FAC | PCSRH0 | 16-bit PPG cycle setting buffer register (upper) ch. 0 | R/W | 0b11111111 |
| 0x0FAD | PCSRL0 | 16-bit PPG cycle setting buffer register (lower) ch. 0 | R/W | 0b11111111 |
| 0x0FAE | PDUTH0 | 16-bit PPG duty setting buffer register (upper) ch. 0 | R/W | 0b11111111 |
| 0x0FAF | PDUTL0 | 16-bit PPG duty setting buffer register (lower) ch. 0 | R/W | 0b11111111 |
| 0x0FB0 | PDCRH1 | 16-bit PPG downcounter register (upper) ch. 1 | R | 0b00000000 |
| 0x0FB1 | PDCRL1 | 16-bit PPG downcounter register (lower) ch. 1 | R | 0b00000000 |
| 0x0FB2 | PCSRH1 | 16-bit PPG cycle setting buffer register (upper) ch. 1 | R/W | 0b11111111 |
| 0x0FB3 | PCSRL1 | 16-bit PPG cycle setting buffer register (lower) ch. 1 | R/W | 0b11111111 |
| 0x0FB4 | PDUTH1 | 16-bit PPG duty setting buffer register (upper) ch. 1 | R/W | 0b11111111 |
| 0x0FB5 | PDUTL1 | 16-bit PPG duty setting buffer register (lower) ch. 1 | R/W | 0b11111111 |
| 0x0FB6 to 0x0FBB | — | (Disabled) | — | — |
| 0x0FBC | BGR1 | LIN-UART baud rate generator register 1 | R/W | 0b00000000 |
| 0x0FBD | BGR0 | LIN-UART baud rate generator register 0 | R/W | 0b00000000 |
| 0x0FBE | PSSR0 | UART/SIO dedicated baud rate generator prescaler select register ch. 0 | R/W | 0b00000000 |
| 0x0FBF | BRSR0 | UART/SIO dedicated baud rate generator baud rate setting register ch. 0 | R/W | 0b00000000 |
| 0x0FC0, 0x0FC1 | — | (Disabled) | — | — |
| 0x0FC2 | AIDRH | A/D input disable register (upper) | R/W | 0b00000000 |
| 0x0FC3 | AIDRL | A/D input disable register (lower) | R/W | 0b00000000 |
| 0x0FC4 | LVDPW | LVD reset circuit password register | R/W | 0b00000000 |
| 0x0FC5 to 0x0FE2 | — | (Disabled) | — | — |
| 0x0FE3 | WCDR | Watch counter data register | R/W | 0b00111111 |
| 0x0FE4 | CRTH | Main CR clock trimming register (upper) | R/W | 0b000XXXXX |
| 0x0FE5 | CRTL | Main CR clock trimming register (lower) | R/W | 0b000XXXXX |
| 0x0FE6 | — | (Disabled) | — | — |
| 0x0FE7 | CRTDA | Main CR clock temperature dependent adjustment register | R/W | 0b000XXXXX |
| 0x0FE8 | SYSC | System configuration register | R/W | 0b11000011 |
| 0x0FE9 | CMCR | Clock monitoring control register | R/W | 0b00000000 |
| 0x0FEA | CMDR | Clock monitoring data register | R | 0b00000000 |
| 0x0FEB | WDTH | Watchdog timer selection ID register (upper) | R | 0bXXXXXXXX |
| 0x0FEC | WDTL | Watchdog timer selection ID register (lower) | R | 0bXXXXXXXX |

*(Continued)*

*(Continued)*

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0x0FED, 0x0FEE | — | (Disabled) | — | — |
| 0x0FEF | WICR | Interrupt pin selection circuit control register | R/W | 0b01000000 |
| 0x0FF0 to 0x0FFF | — | (Disabled) | — | — |

- R/W access symbols
  R/W : Readable/Writable
  R : Read only
- Initial value symbols
  0 : The initial value of this bit is “0”.
  1 : The initial value of this bit is “1”.
  X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

## ■ I/O PORTS

• List of port registers

| Register name | | Read/Write | Initial value |
|---|---|---|---|
| Port 0 data register | PDR0 | R, RM/W | 0b00000000 |
| Port 0 direction register | DDR0 | R/W | 0b00000000 |
| Port 1 data register | PDR1 | R, RM/W | 0b00000000 |
| Port 1 direction register | DDR1 | R/W | 0b00000000 |
| Port 2 data register | PDR2 | R, RM/W | 0b00000000 |
| Port 2 direction register | DDR2 | R/W | 0b00000000 |
| Port 3 data register | PDR3 | R, RM/W | 0b00000000 |
| Port 3 direction register | DDR3 | R/W | 0b00000000 |
| Port 4 data register | PDR4 | R, RM/W | 0b00000000 |
| Port 4 direction register | DDR4 | R/W | 0b00000000 |
| Port 5 data register | PDR5 | R, RM/W | 0b00000000 |
| Port 5 direction register | DDR5 | R/W | 0b00000000 |
| Port 6 data register | PDR6 | R, RM/W | 0b00000000 |
| Port 6 direction register | DDR6 | R/W | 0b00000000 |
| Port 7 data register | PDR7 | R, RM/W | 0b00000000 |
| Port 7 direction register | DDR7 | R/W | 0b00000000 |
| Port 8 data register | PDR8 | R, RM/W | 0b00000000 |
| Port 8 direction register | DDR8 | R/W | 0b00000000 |
| Port E data register | PDRE | R, RM/W | 0b00000000 |
| Port E direction register | DDRE | R/W | 0b00000000 |
| Port F data register | PDRF | R, RM/W | 0b00000000 |
| Port F direction register | DDRF | R/W | 0b00000000 |
| Port G data register | PDRG | R, RM/W | 0b00000000 |
| Port G direction register | DDRG | R/W | 0b00000000 |
| Port 0 pull-up register | PUL0 | R/W | 0b00000000 |
| Port 1 pull-up register | PUL1 | R/W | 0b00000000 |
| Port 2 pull-up register | PUL2 | R/W | 0b00000000 |
| Port 3 pull-up register | PUL3 | R/W | 0b00000000 |
| Port 4 pull-up register | PUL4 | R/W | 0b00000000 |
| Port 5 pull-up register | PUL5 | R/W | 0b00000000 |
| Port 6 pull-up register | PUL6 | R/W | 0b00000000 |
| Port 7 pull-up register | PUL7 | R/W | 0b00000000 |
| Port 8 pull-up register | PUL8 | R/W | 0b00000000 |
| Port E pull-up register | PULE | R/W | 0b00000000 |
| Port G pull-up register | PULG | R/W | 0b00000000 |
| A/D input disable register (upper) | AIDRH | R/W | 0b00000000 |
| A/D input disable register (lower) | AIDRL | R/W | 0b00000000 |

R/W : Readable/writable (The read value is the same as the write value.)
R, RM/W : Readable/writable (The read value is different from the write value. The write value is read by the read-modify-write (RMW) type of instruction.)

### 1. Port 0

Port 0 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95810K Series Hardware Manual”.

#### (1) Port 0 configuration

Port 0 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 0 data register (PDR0)
- Port 0 direction register (DDR0)
- Port 0 pull-up register (PUL0)

#### (2) Block diagrams of port 0

- P00/INT00 pin
  This pin has the following peripheral function:
  - External interrupt input pin (INT00)

- P01/INT01 pin
  This pin has the following peripheral function:
  - External interrupt input pin (INT01)

- P02/INT02 pin
  This pin has the following peripheral function:
  External interrupt input pin (INT02)

- P03/INT03 pin
  This pin has the following peripheral function:
  - External interrupt input pin (INT03)

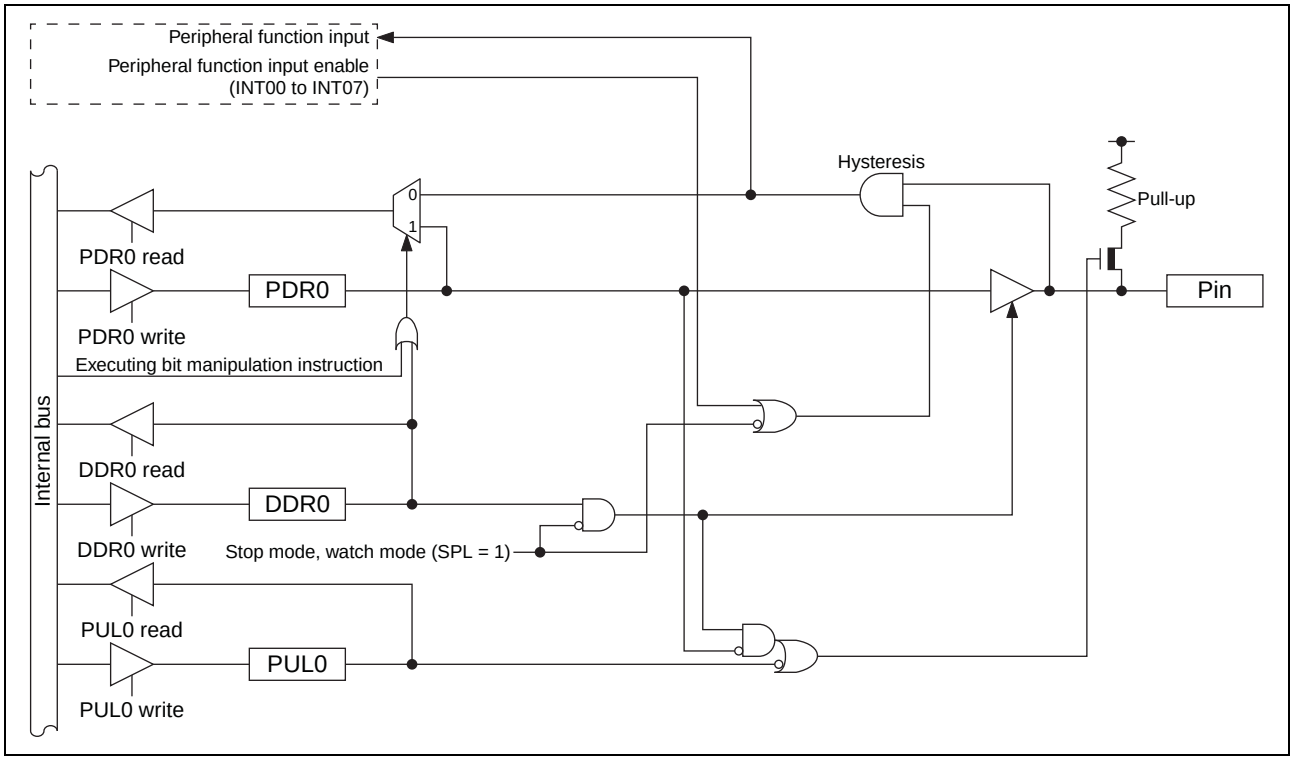
- P04/INT04 pin
  This pin has the following peripheral function:
  - External interrupt input pin (INT04)

- P05/INT05 pin
  This pin has the following peripheral function:
  - External interrupt input pin (INT05)

- P06/INT06 pin
  This pin has the following peripheral function:
  - External interrupt input pin (INT06)

- P07/INT07 pin
  This pin has the following peripheral function:
  - External interrupt input pin (INT07)

- Block diagram of P00/INT00, P01/INT01, P02/INT02, P03/INT03, P04/INT04, P05/INT05, P06/INT06 and P07/INT07



### (3) Port 0 registers

• Port 0 register functions

| Register abbreviation | Data | Read | Read by read-modify-write (RMW) instruction | Write |
|---|---|---|---|---|
| PDR0 | 0 | Pin state is “L” level. | PDR0 value is “0”. | As output port, outputs “L” level. |
| | 1 | Pin state is “H” level. | PDR0 value is “1”. | As output port, outputs “H” level. |
| DDR0 | 0 | Port input enabled | | |
| | 1 | Port output enabled | | |
| PUL0 | 0 | Pull-up disabled | | |
| | 1 | Pull-up enabled | | |

• Correspondence between registers and pins for port 0

| | Correspondence between related register bits and pins | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Pin name | P07 | P06 | P05 | P04 | P03 | P02 | P01 | P00 |
| PDR0 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| DDR0 | | | | | | | | |
| PUL0 | | | | | | | | |

**(4) Port 0 operations**

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR0 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR0 register to external pins.
  - If data is written to the PDR0 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR0 register returns the PDR0 register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR0 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR0 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR0 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR0 register corresponding to the input pin of a peripheral function to “0”.
  - Reading the PDR0 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDR0 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR0 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input is enabled for the external interrupt (INT00 to INT07), the input is enabled and not blocked.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation as an external interrupt input pin
  - Set the bit in the DDR0 register corresponding to the external interrupt input pin to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - The pin value is always input to the external interrupt circuit. When using a pin for a function other than the interrupt, disable the external interrupt function corresponding to that pin.

- Operation of the pull-up register
  Setting the bit in the PUL0 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL0 register.

## 2. Port 1

Port 1 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95810K Series Hardware Manual”.

### (1) Port 1 configuration

Port 1 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 1 data register (PDR1)
- Port 1 direction register (DDR1)
- Port 1 pull-up register (PUL1)

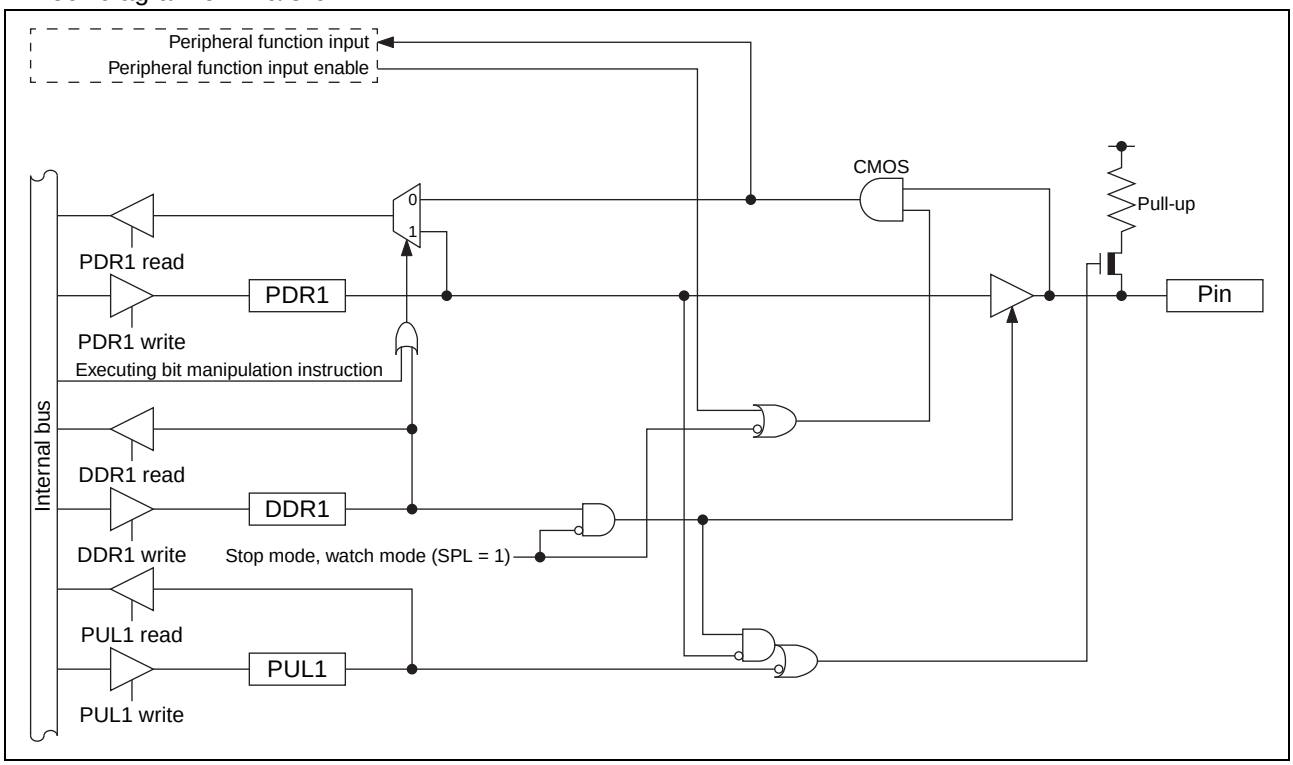
### (2) Block diagrams of port 1

- P10/UI0 pin

  This pin has the following peripheral function:

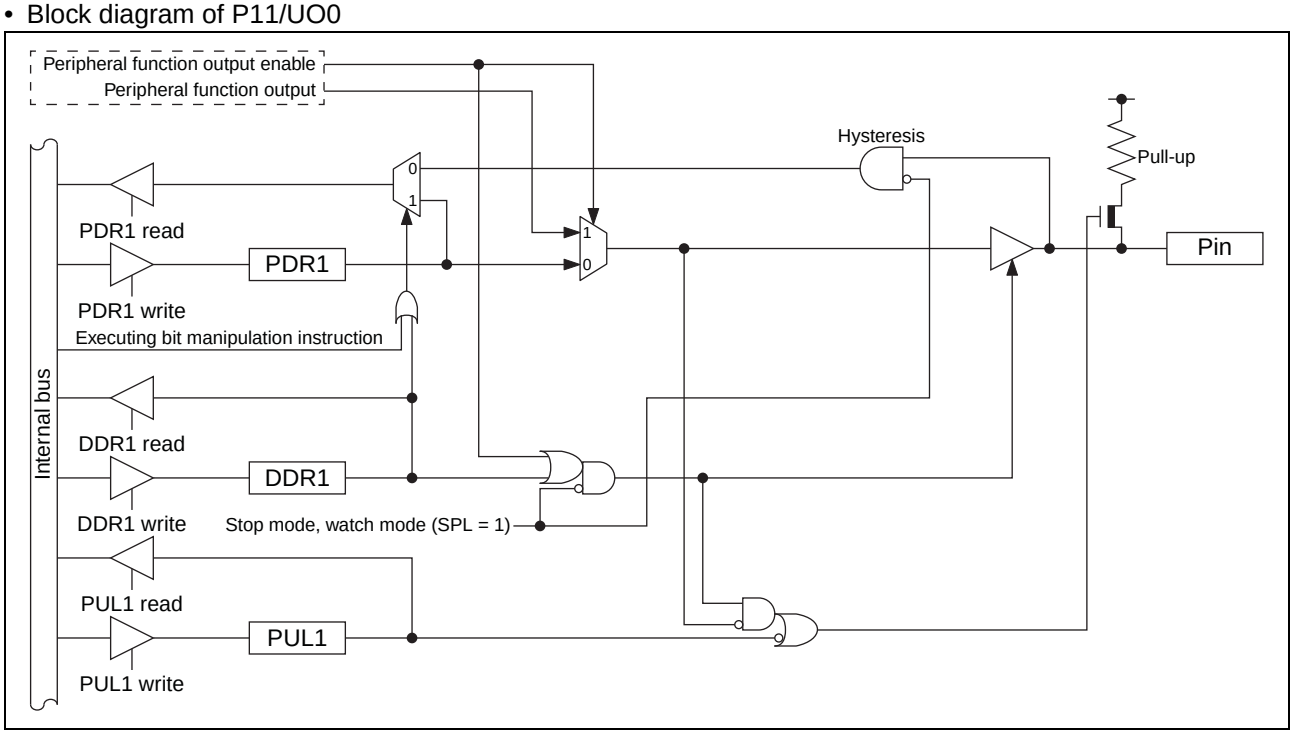
  - UART/SIO ch. 0 data input pin (UI0)

- Block diagram of P10/UI0



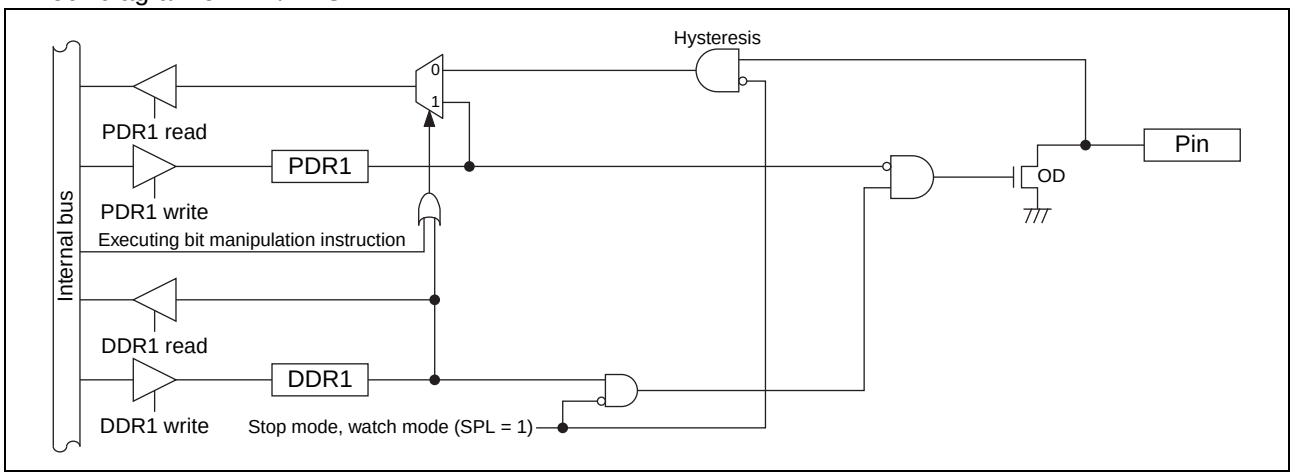
- P11/UO0 pin
  This pin has the following peripheral function:
  - UART/SIO ch. 0 data output pin (UO0)

- Block diagram of P11/UO0




- P12/DBG pin
  This pin has the following peripheral function:
  - DBG input pin (DBG)

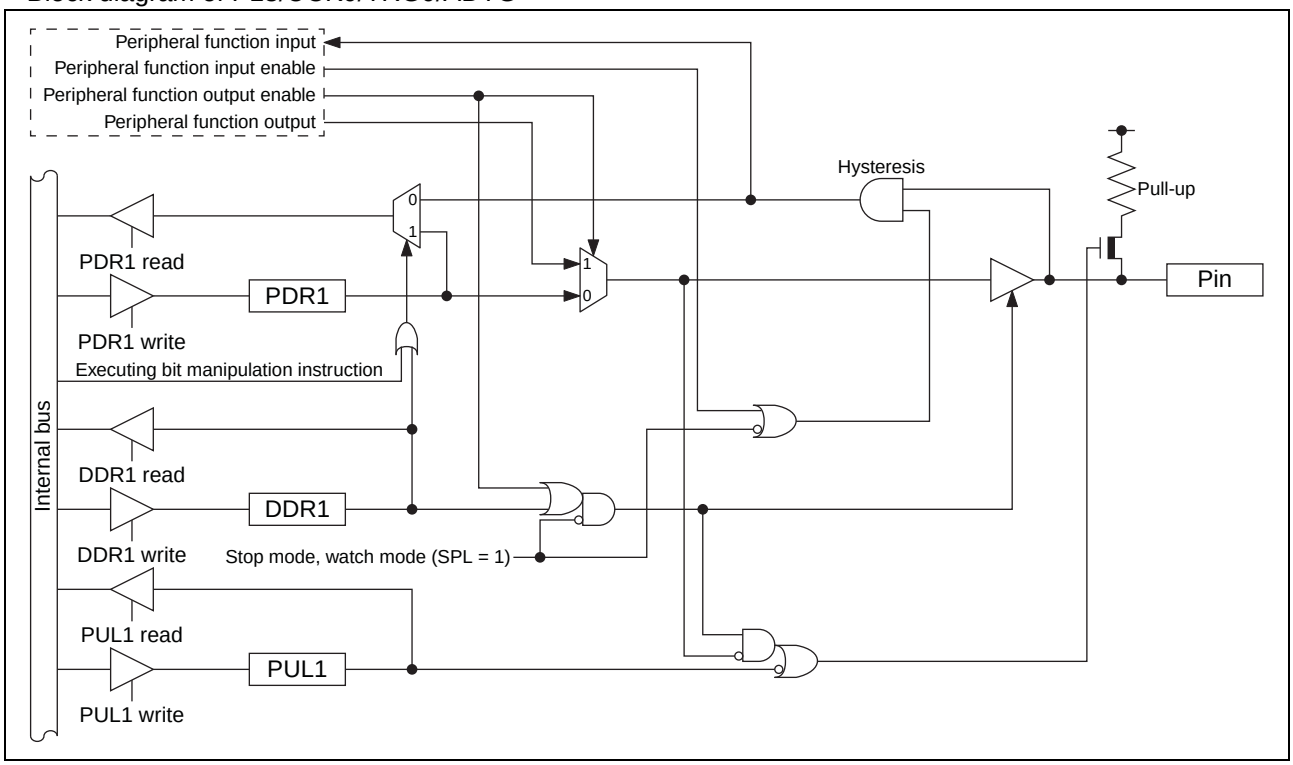
- Block diagram of P12/DBG



- P13/UCK0/TRG0/ADTG* pin
  This pin has the following peripheral functions:
  - UART/SIO ch. 0 clock I/O pin (UCK0)
  - 16-bit PPG timer ch. 0 trigger input pin (TRG0)
  - 8/10-bit A/D converter trigger input pin (ADTG)

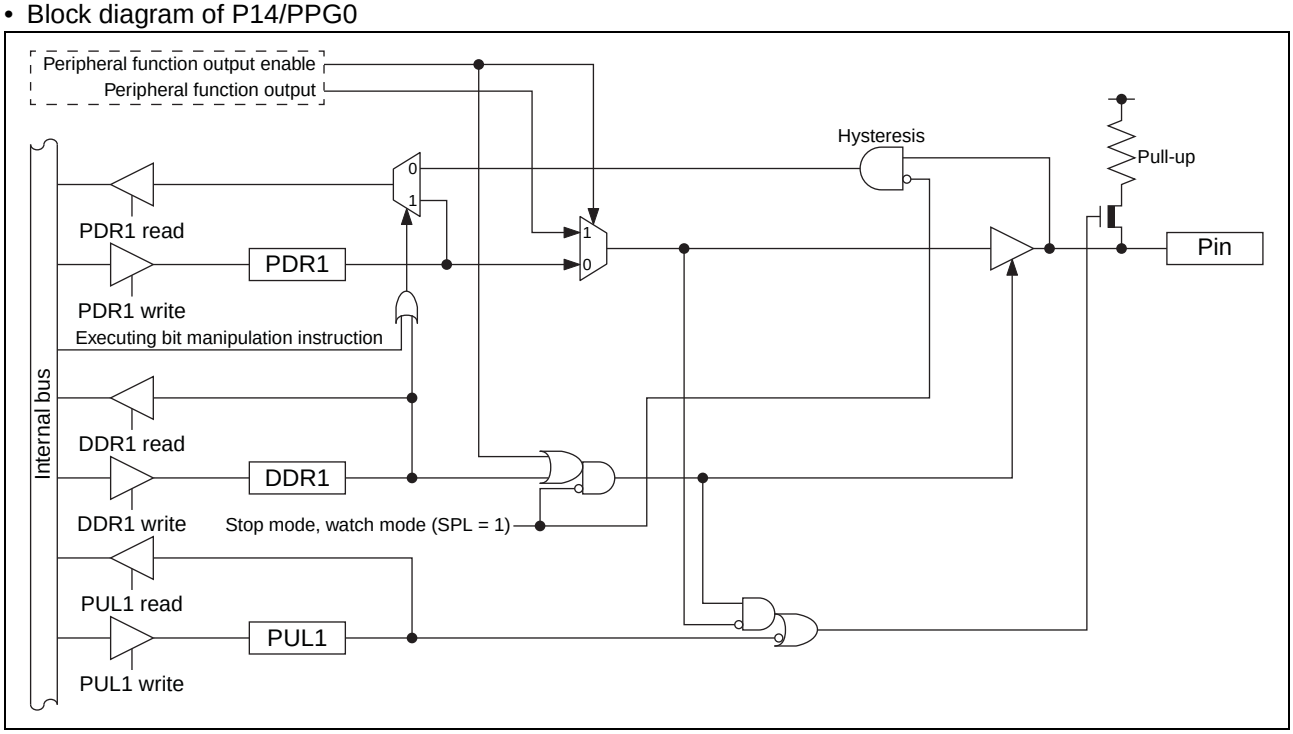
*: TRG0 and ADTG can be mapped to either P13 or P83 by using the SYSC register.

- Block diagram of P13/UCK0/TRG0/ADTG



- P14/PPG0 pin
  This pin has the following peripheral function:
  - 16-bit PPG timer ch. 0 output pin (PPG0)

- Block diagram of P14/PPG0



### (3) Port 1 registers

• Port 1 register functions

| Register abbreviation | Data | Read | Read by read-modify-write (RMW) instruction | Write |
|---|---|---|---|---|
| PDR1 | 0 | Pin state is “L” level. | PDR1 value is “0”. | As output port, outputs “L” level. |
| | 1 | Pin state is “H” level. | PDR1 value is “1”. | As output port, outputs “H” level.* |
| DDR1 | 0 | Port input enabled | | |
| | 1 | Port output enabled | | |
| PUL1 | 0 | Pull-up disabled | | |
| | 1 | Pull-up enabled | | |

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

• Correspondence between registers and pins for port 1

| | Correspondence between related register bits and pins | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Pin name** | **-** | **-** | **-** | **P14** | **P13** | **P12** | **P11** | **P10** |
| PDR1 | - | - | - | bit4 | bit3 | bit2* | bit1 | bit0 |
| DDR1 | | | | | | | | |
| PUL1 | | | | | | | | |

*: Though P12 has no pull-up function, bit2 in the PUL1 register can still be accessed. The operation of P12 is not affected by the setting of bit2 in the PUL1 register.

**(4) Port 1 operations**

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR1 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR1 register to external pins.
  - If data is written to the PDR1 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR1 register returns the PDR1 register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR1 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR1 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR1 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDR1 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR1 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR1 register corresponding to the input pin of a peripheral function to “0”.
  - Reading the PDR1 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDR1 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR1 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input of P10/UI0 and P13/UCK0/TRG0/ADTG is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PUL1 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL1 register.

### 3. Port 2

Port 2 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95810K Series Hardware Manual”.

#### (1) Port 2 configuration

Port 2 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 2 data register (PDR2)
- Port 2 direction register (DDR2)
- Port 2 pull-up register (PUL2)

#### (2) Block diagrams of port 2

- P20/PPG00 pin

  This pin has the following peripheral function:
  - 8/16-bit PPG ch. 0 output pin (PPG00)

- P21/PPG01 pin

  This pin has the following peripheral function:
  - 8/16-bit PPG ch. 0 output pin (PPG01)

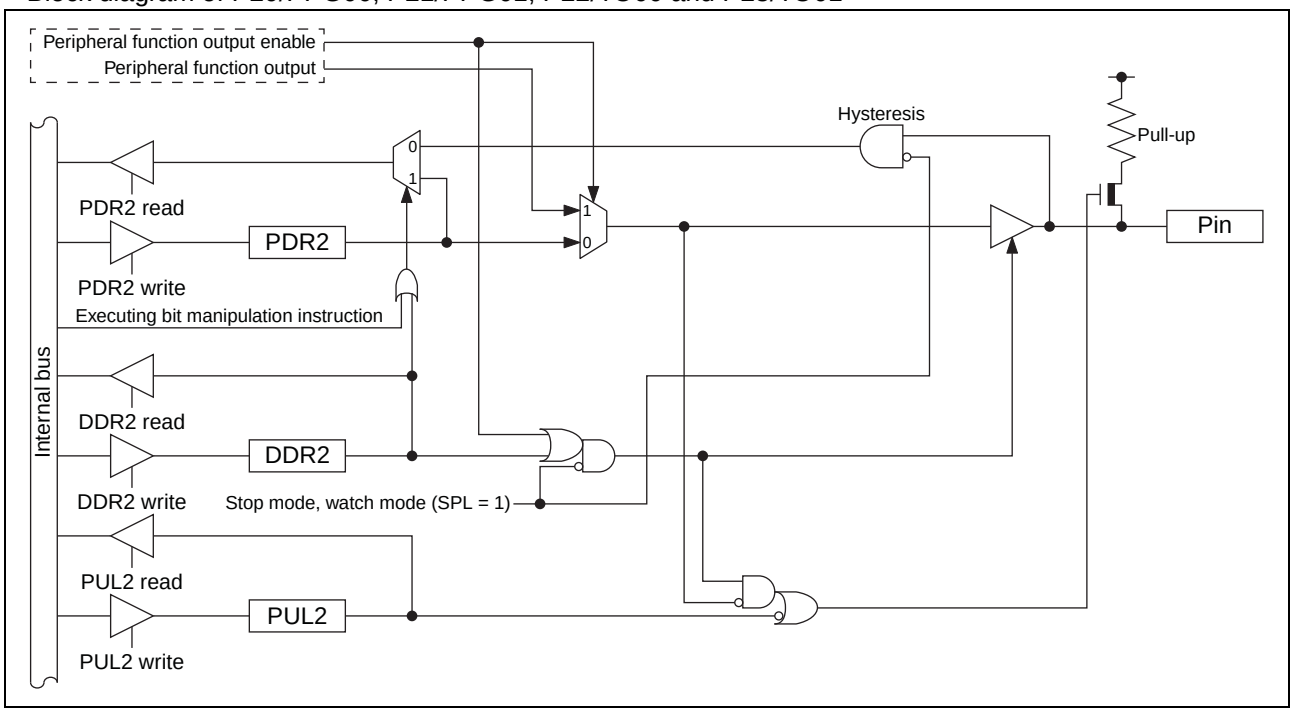
- P22/TO00 pin

  This pin has the following peripheral function:
  - 8/16-bit composite timer ch. 0 output pin (TO00)

- P23/TO01 pin

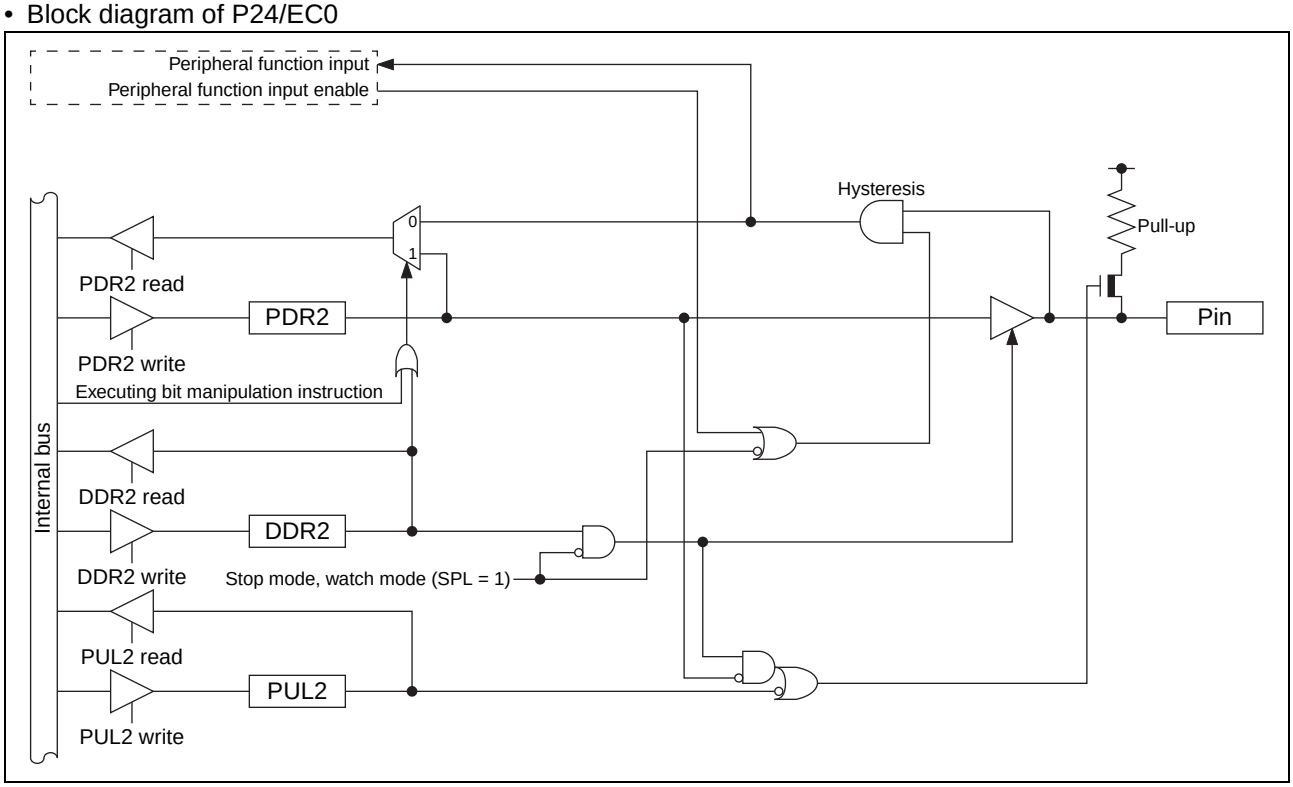
  This pin has the following peripheral function:
  - 8/16-bit composite timer ch. 0 output pin (TO01)

- Block diagram of P20/PPG00, P21/PPG01, P22/TO00 and P23/TO01



- P24/EC0 pin
  This pin has the following peripheral function:
  - 8/16-bit composite timer ch. 0 clock input pin (EC0)

- Block diagram of P24/EC0



### (3) Port 2 registers

• Port 2 register functions

| Register abbreviation | Data | Read | Read by read-modify-write (RMW) instruction | Write |
|---|---|---|---|---|
| PDR2 | 0 | Pin state is “L” level. | PDR2 value is “0”. | As output port, outputs “L” level. |
| | 1 | Pin state is “H” level. | PDR2 value is “1”. | As output port, outputs “H” level. |
| DDR2 | 0 | Port input enabled | | |
| | 1 | Port output enabled | | |
| PUL2 | 0 | Pull-up disabled | | |
| | 1 | Pull-up enabled | | |

• Correspondence between registers and pins for port 2

| | Correspondence between related register bits and pins | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Pin name** | **-** | **-** | **-** | **P24** | **P23** | **P22** | **P21** | **P20** |
| PDR2 | - | - | - | bit4 | bit3 | bit2 | bit1 | bit0 |
| DDR2 | | | | | | | | |
| PUL2 | | | | | | | | |

**(4) Port 2 operations**

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR2 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR2 register to external pins.
  - If data is written to the PDR2 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR2 register returns the PDR2 register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR2 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR2 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR2 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR2 register, the PDR2 register value is returned.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDR2 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR2 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR2 register, the PDR2 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR2 register corresponding to the input pin of a peripheral function to “0”.
  - Reading the PDR2 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR2 register, the PDR2 register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDR2 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR2 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input of P24/EC0 is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PUL2 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL2 register.

### 4. Port 3

Port 3 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95810K Series Hardware Manual”.

#### (1) Port 3 configuration

Port 3 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 3 data register (PDR3)
- Port 3 direction register (DDR3)
- Port 3 pull-up register (PUL3)
- A/D input disable register (lower) (AIDRL)

**(2) Block diagrams of port 3**

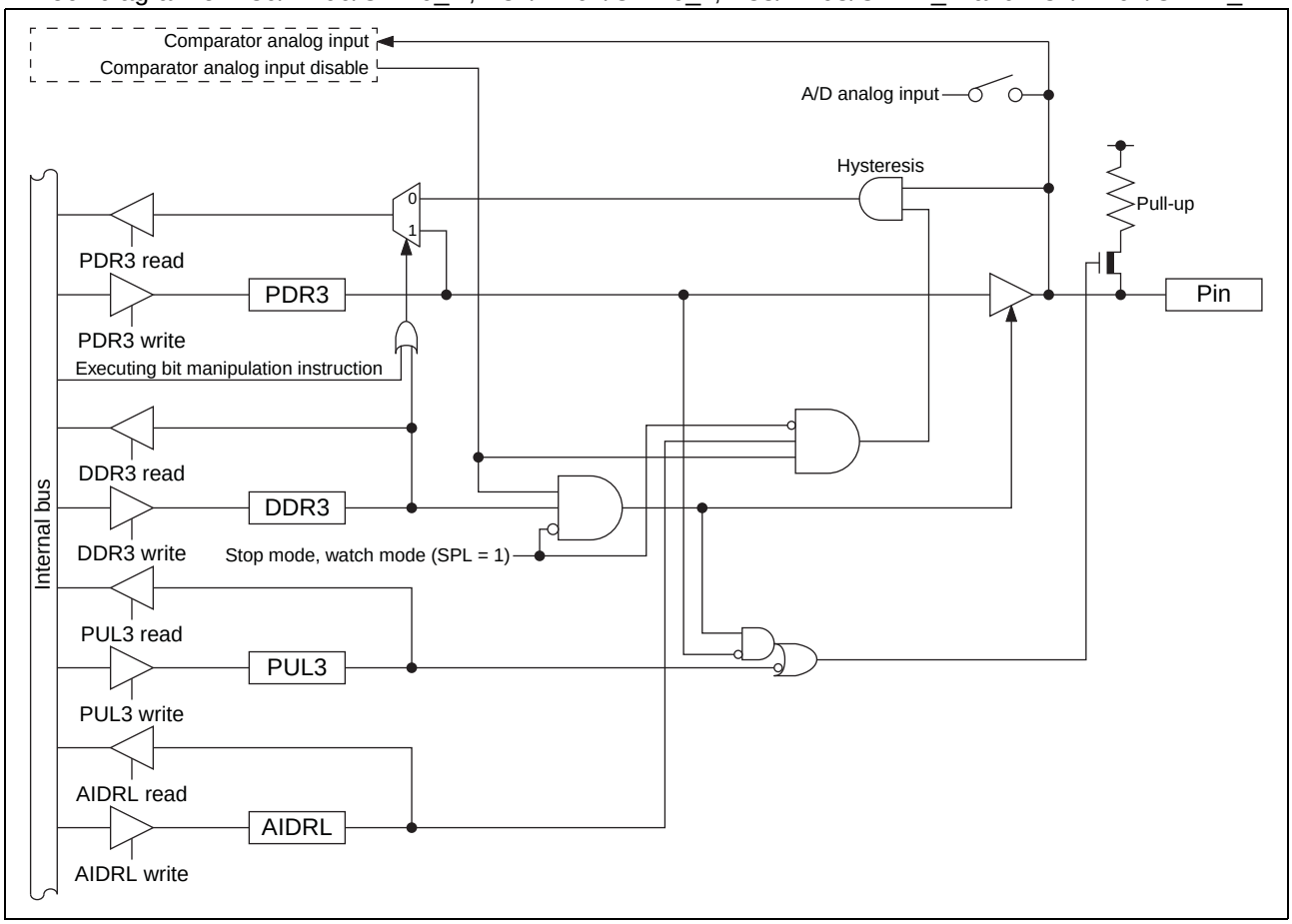
- P30/AN00/CMP0_N pin
  This pin has the following peripheral functions:
  - 8/10-bit A/D converter analog input pin (AN00)
  - Comparator ch. 0 inverting analog input (negative input) pin (CMP0_N)

- P31/AN01/CMP0_P pin
  This pin has the following peripheral functions:
  - 8/10-bit A/D converter analog input pin (AN01)
  - Comparator ch. 0 non-inverting analog input (positive input) pin (CMP0_P)

- P33/AN03/CMP1_N pin
  This pin has the following peripheral functions:
  - 8/10-bit A/D converter analog input pin (AN03)
  - Comparator ch. 1 inverting analog input (negative input) pin (CMP1_N)

- P34/AN04/CMP1_P pin
  This pin has the following peripheral functions:
  - 8/10-bit A/D converter analog input pin (AN04)
  - Comparator ch. 1 non-inverting analog input (positive input) pin (CMP1_P)

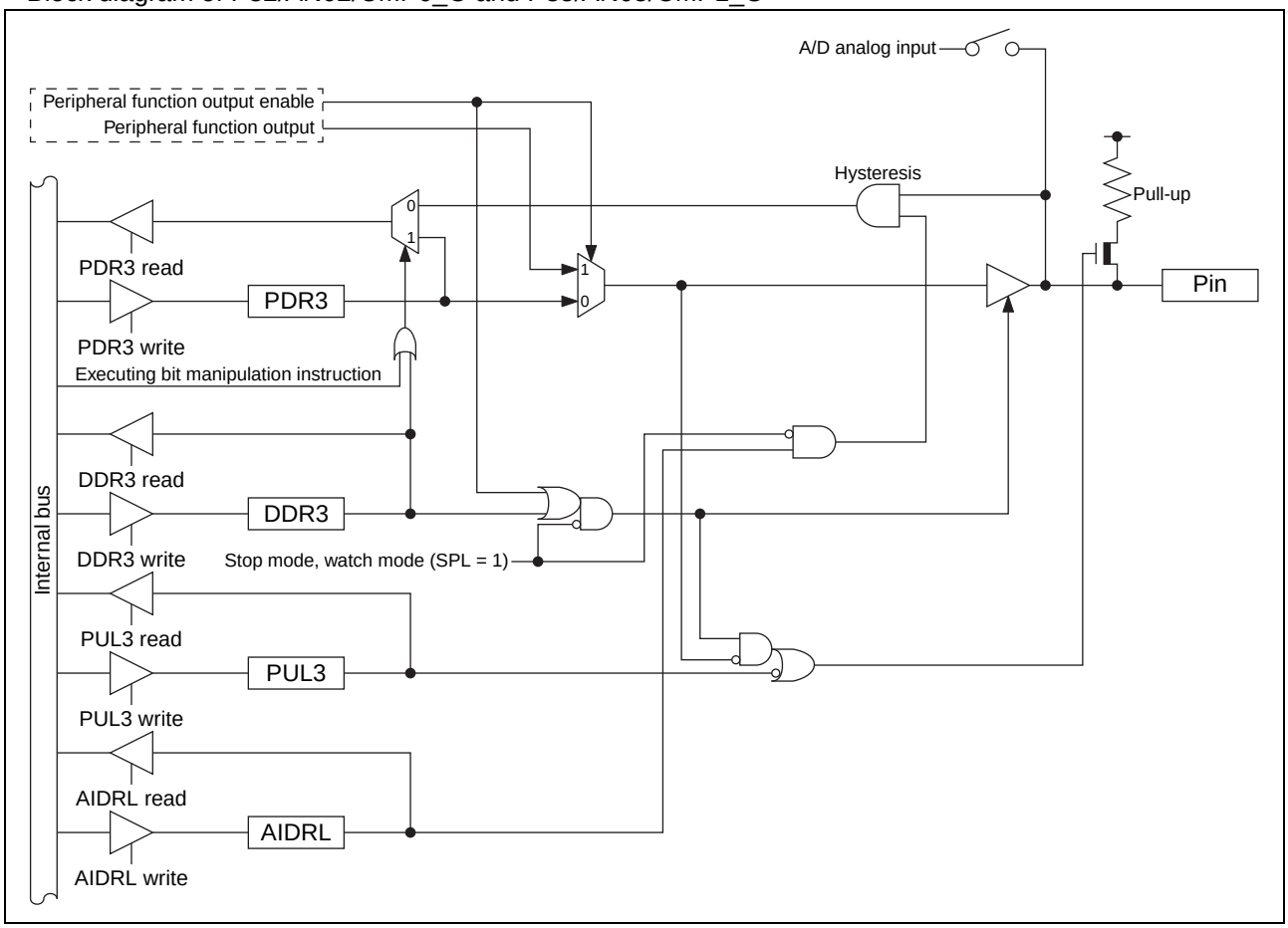
- Block diagram of P30/AN00/CMP0_N, P31/AN01/CMP0_P, P33/AN03/CMP1_N and P34/AN04/CMP1_P



- P32/AN02/CMP0_O pin
  This pin has the following peripheral functions:
  - 8/10-bit A/D converter analog input pin (AN02)
  - Comparator ch. 0 digital output pin (CMP0_O)

- P35/AN05/CMP1_O pin
  This pin has the following peripheral functions:
  - 8/10-bit A/D converter analog input pin (AN05)
  - Comparator ch. 1 digital output pin (CMP1_O)

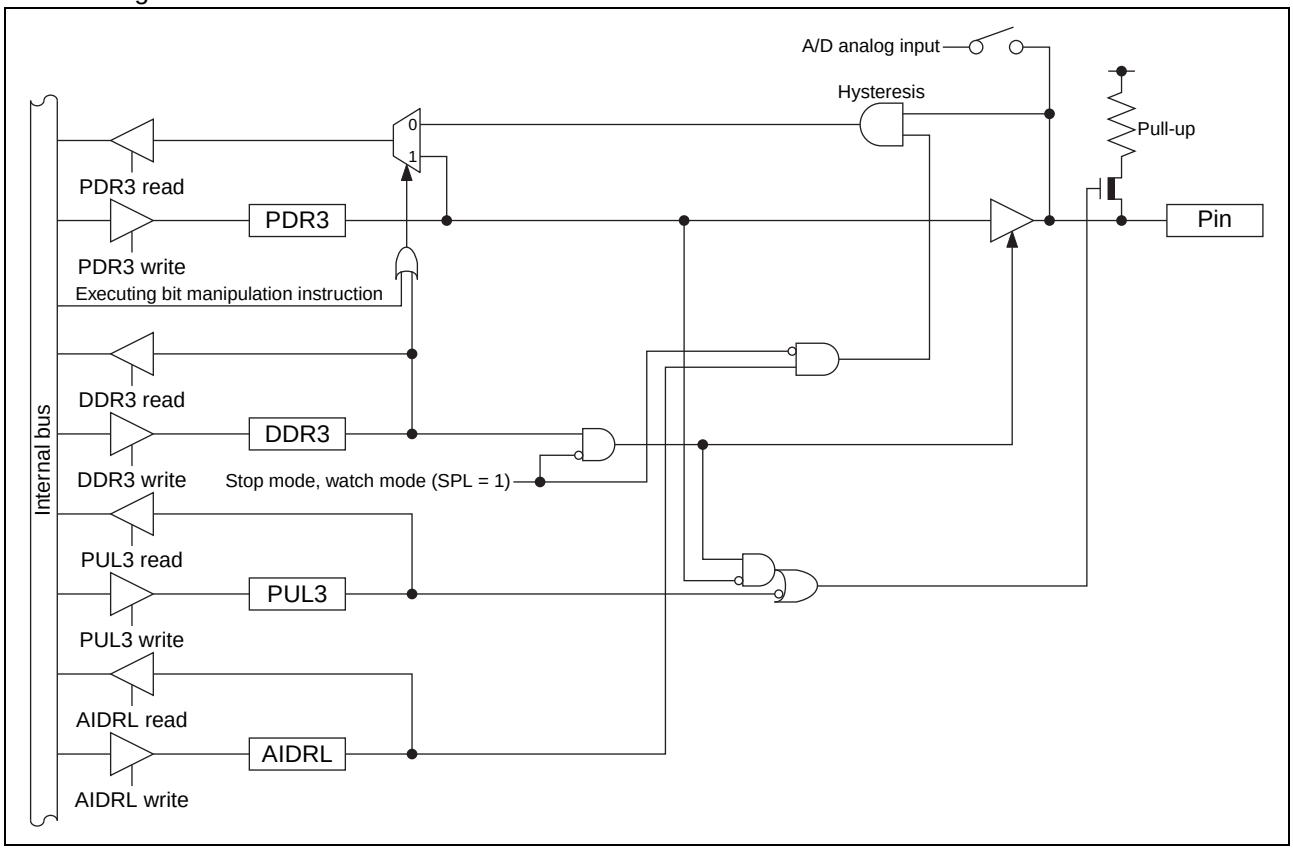
- Block diagram of P32/AN02/CMP0_O and P35/AN05/CMP1_O



- P36/AN06 pin
  This pin has the following peripheral function:
  - 8/10-bit A/D converter analog input pin (AN06)

- P37/AN07 pin
  This pin has the following peripheral function:
  - 8/10-bit A/D converter analog input pin (AN07)

- Block diagram of P36/AN06 and P37/AN07



### (3) Port 3 registers

• Port 3 register functions

| Register abbreviation | Data | Read | Read by read-modify-write (RMW) instruction | Write |
|---|---|---|---|---|
| PDR3 | 0 | Pin state is “L” level. | PDR3 value is “0”. | As output port, outputs “L” level. |
| | 1 | Pin state is “H” level. | PDR3 value is “1”. | As output port, outputs “H” level. |
| DDR3 | 0 | Port input enabled | | |
| | 1 | Port output enabled | | |
| PUL3 | 0 | Pull-up disabled | | |
| | 1 | Pull-up enabled | | |
| AIDRL | 0 | Analog input enabled | | |
| | 1 | Port input enabled | | |

• Correspondence between registers and pins for port 3

| | Correspondence between related register bits and pins | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Pin name | P37 | P36 | P35 | P34 | P33 | P32 | P31 | P30 |
| PDR3 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| DDR3 | | | | | | | | |
| PUL3 | | | | | | | | |
| AIDRL | | | | | | | | |

**(4) Port 3 operations**

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR3 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR3 register to external pins.
  - If data is written to the PDR3 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR3 register returns the PDR3 register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR3 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When using a pin shared with the analog input function as an input port, set the corresponding bit in the A/D input disable register (lower) (AIDRL) to “1”.
  - If data is written to the PDR3 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR3 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR3 register, the PDR3 register value is returned.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDR3 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR3 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR3 register, the PDR3 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR3 register corresponding to the input pin of a peripheral function to “0”.
  - When using a pin shared with the analog input function as another peripheral function input pin, configure it as an input port by setting the bit in the AIDRL register corresponding to that pin to “1”.
  - Reading the PDR3 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR3 register, the PDR3 register value is returned.

- Operation at reset

  If the CPU is reset, all bits in the DDR3 register are initialized to “0” and port input is enabled. As for a pin shared with the analog input function, its port input is disabled because the AIDRL register is initialized to “0”.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR3 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation as an analog input pin
  - Set the bit in the DDR3 register bit corresponding to the analog input pin to “0” and the bit corresponding to that pin in the AIDRL register to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions. In addition, set the corresponding bit in the PUL3 register to “0”.

- Operation of the pull-up register
  Setting the bit in the PUL3 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL3 register.

- Operation as a comparator input pin (only for P31 and P34)
  - Set the bit in the AIDRL register corresponding to the comparator input pin to “0”.
  - Regardless of the value of the PDR3 register and that of the DDR3 register, if the comparator analog input enable bit in the comparator control register ch. 0/ch. 1 (CMR0/CMR1:VCID) is set to “0”, the comparator input function is enabled.
  - To disable the comparator input function, set the VCID bit to “1”.
  - For details of the comparator, refer to “CHAPTER 28 COMPARATOR” in “New 8FX MB95810K Series Hardware Manual”.

- Operation as a comparator input pin (only for P30 and P33)
  - Set the bit in the AIDRL register corresponding to the comparator input pin to “0”.
  - Regardless of the value of the PDR3 register and that of the DDR3 register, if the comparator analog input enable bit (VCID) and the negative analog input voltage source select bit (BGRS) in the comparator control register ch. 0/ch. 1 (CMR0/CMR1) are both set to “0”, the comparator input function is enabled.
  - To disable the comparator input function, set the VCID bit or the BGRS bit to “1”.
  - For details of the comparator, refer to “CHAPTER 28 COMPARATOR” in “New 8FX MB95810K Series Hardware Manual”.

## 5. Port 4

Port 4 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95810K Series Hardware Manual”.

### (1) Port 4 configuration

Port 4 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 4 data register (PDR4)
- Port 4 direction register (DDR4)
- Port 4 pull-up register (PUL4)
- A/D input disable register (upper) (AIDRH)

### (2) Block diagrams of port 4

- P40/AN08 pin

  This pin has the following peripheral function:
  - 8/10-bit A/D converter analog input pin (AN08)

- P41/AN09 pin

  This pin has the following peripheral function:
  - 8/10-bit A/D converter analog input pin (AN09)

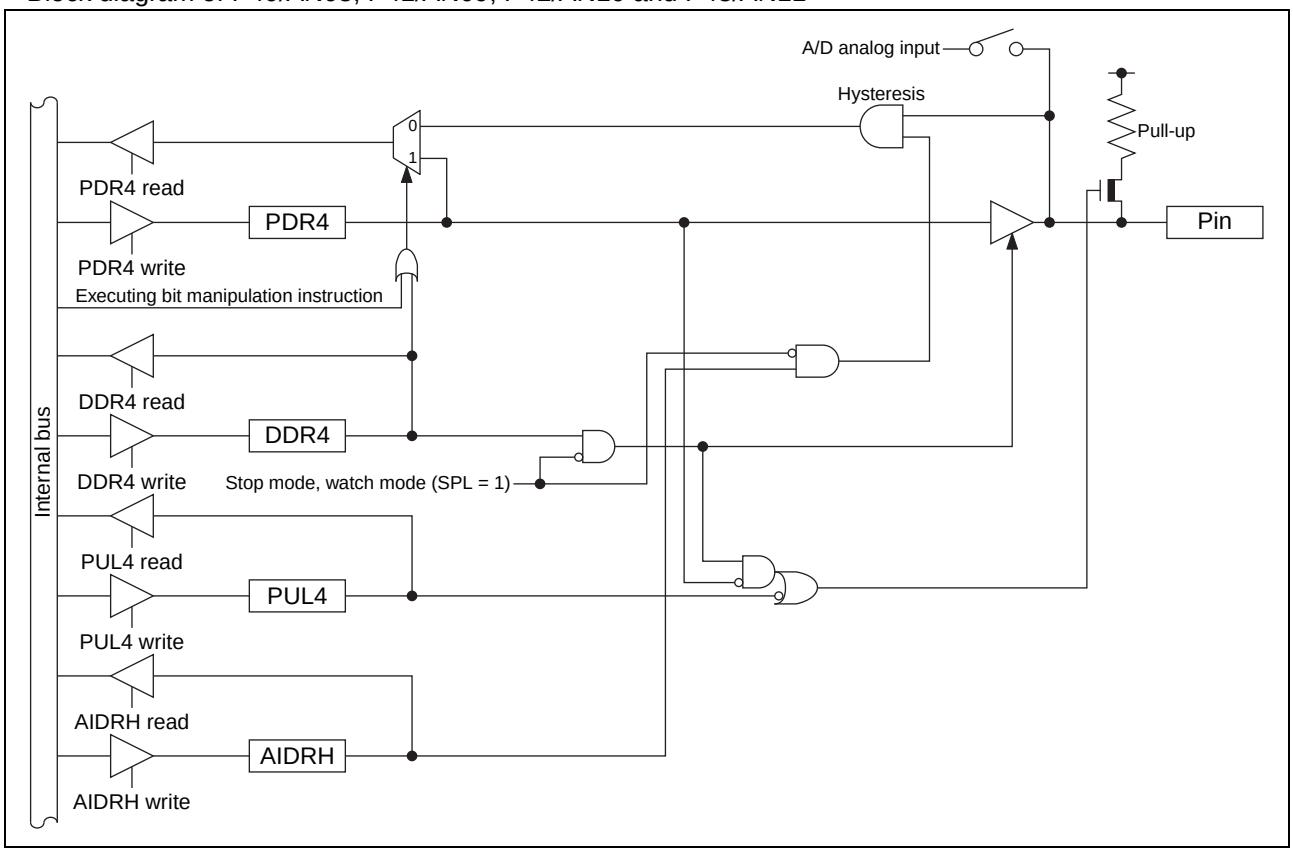
- P42/AN10 pin

  This pin has the following peripheral function:
  - 8/10-bit A/D converter analog input pin (AN10)

- P43/AN11 pin

  This pin has the following peripheral function:
  - 8/10-bit A/D converter analog input pin (AN11)

- Block diagram of P40/AN08, P41/AN09, P42/AN10 and P43/AN11



### (3) Port 4 registers

• Port 4 register functions

| Register abbreviation | Data | Read | Read by read-modify-write (RMW) instruction | Write |
|---|---|---|---|---|
| PDR4 | 0 | Pin state is “L” level. | PDR4 value is “0”. | As output port, outputs “L” level. |
| | 1 | Pin state is “H” level. | PDR4 value is “1”. | As output port, outputs “H” level. |
| DDR4 | 0 | Port input enabled | | |
| | 1 | Port output enabled | | |
| PUL4 | 0 | Pull-up disabled | | |
| | 1 | Pull-up enabled | | |
| AIDRH | 0 | Analog input enabled | | |
| | 1 | Port input enabled | | |

• Correspondence between registers and pins for port 4

| | Correspondence between related register bits and pins | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Pin name** | **-** | **-** | **-** | **-** | **P43** | **P42** | **P41** | **P40** |
| PDR4 | - | - | - | - | bit3 | bit2 | bit1 | bit0 |
| DDR4 | | | | | | | | |
| PUL4 | | | | | | | | |
| AIDRH | | | | | | | | |

**(4) Port 4 operations**

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR4 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR4 register to external pins.
  - If data is written to the PDR4 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR4 register returns the PDR4 register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR4 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When using a pin shared with the analog input function as an input port, set the corresponding bit in the A/D input disable register (upper) (AIDRH) to “1”.
  - If data is written to the PDR4 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR4 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR4 register corresponding to the input pin of a peripheral function to “0”.
  - When using a pin shared with the analog input function as another peripheral function input pin, configure it as an input port by setting the bit in the AIDRH register corresponding to that pin to “1”.
  - Reading the PDR4 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDR4 register are initialized to “0” and port input is enabled. As for a pin shared with the analog input function, its port input is disabled because the AIDRH register is initialized to “0”.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR4 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation as an analog input pin
  - Set the bit in the DDR4 register bit corresponding to the analog input pin to “0” and the bit corresponding to that pin in the AIDRH register to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions. In addition, set the corresponding bit in the PUL4 register to “0”.

- Operation of the pull-up register
  Setting the bit in the PUL4 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL4 register.

## 6. Port 5

Port 5 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95810K Series Hardware Manual”.

### (1) Port 5 configuration

Port 5 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 5 data register (PDR5)
- Port 5 direction register (DDR5)
- Port 5 pull-up register (PUL5)

### (2) Block diagrams of port 5

- P50/SCL pin

  This pin has the following peripheral function:

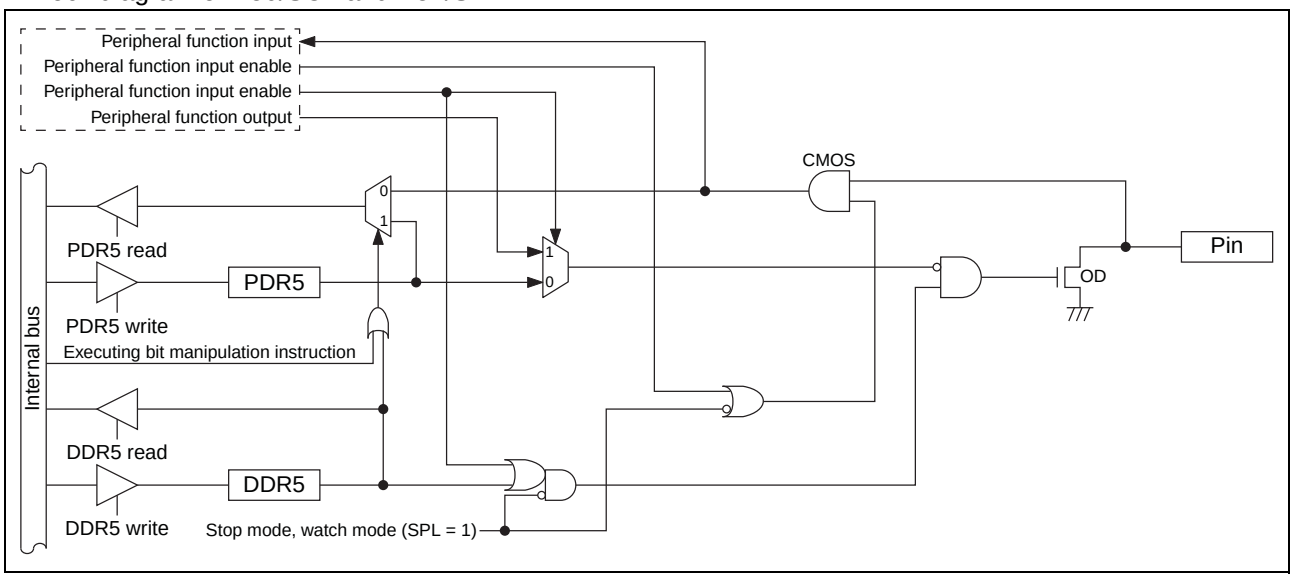
  - I²C bus interface ch. 0 clock I/O pin (SCL)

- P51/SDA pin

  This pin has the following peripheral function:

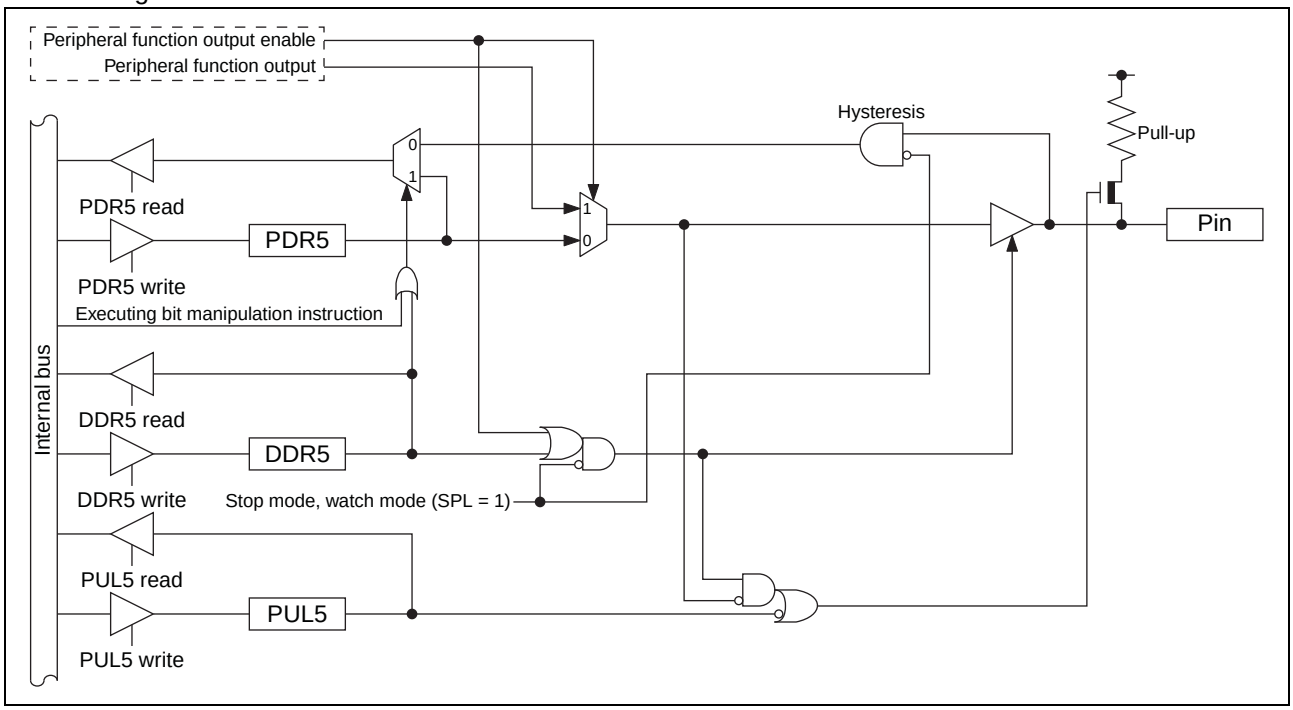
  - I²C bus interface ch. 0 data I/O pin (SDA)

- Block diagram of P50/SCL and P51/SDA



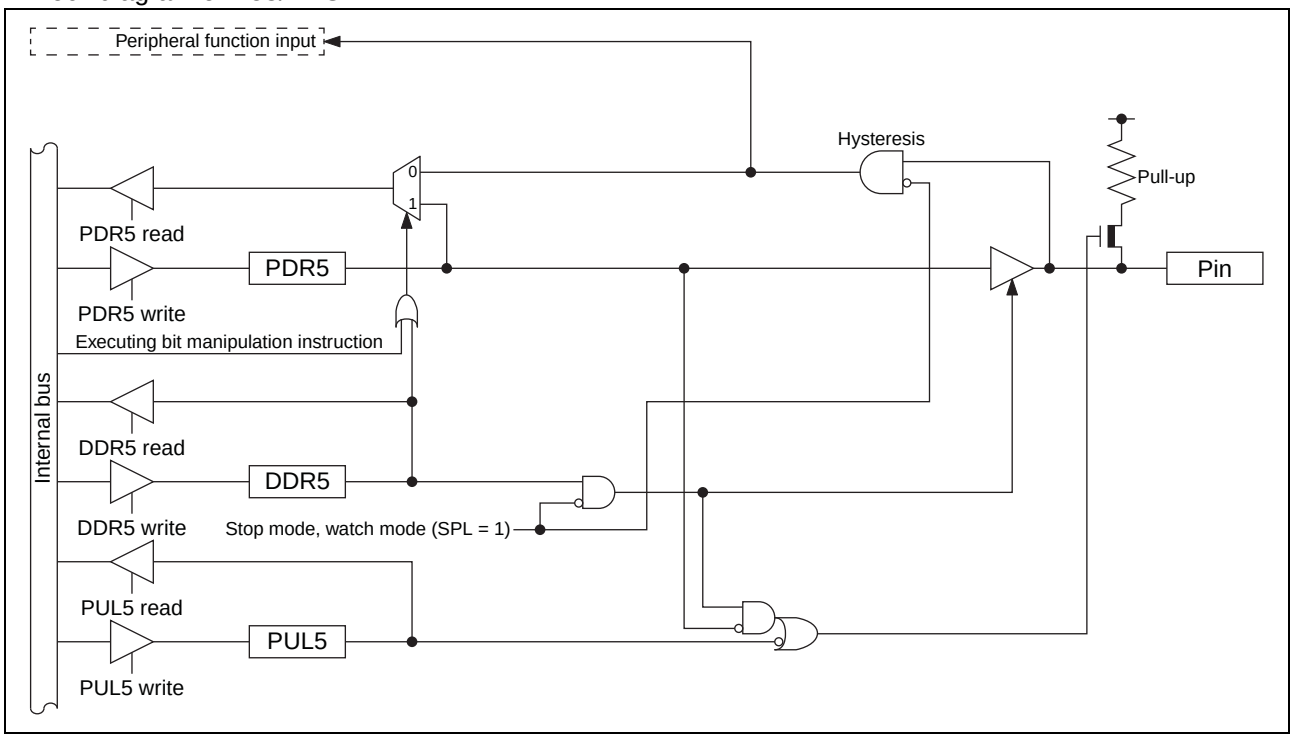
- P52/PPG1 pin
  This pin has the following peripheral function:
  - 16-bit PPG timer ch. 1 output pin (PPG1)

- Block diagram of P52/PPG1




- P53/TRG1 pin
  This pin has the following peripheral function:
  - 16-bit PPG timer ch. 1 trigger input pin (TRG1)

- Block diagram of P53/TRG1



### (3) Port 5 registers

• Port 5 register functions

| Register abbreviation | Data | Read | Read by read-modify-write (RMW) instruction | Write |
|---|---|---|---|---|
| PDR5 | 0 | Pin state is “L” level. | PDR5 value is “0”. | As output port, outputs “L” level. |
| | 1 | Pin state is “H” level. | PDR5 value is “1”. | As output port, outputs “H” level.* |
| DDR5 | 0 | Port input enabled | | |
| | 1 | Port output enabled | | |
| PUL5 | 0 | Pull-up disabled | | |
| | 1 | Pull-up enabled | | |

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

• Correspondence between registers and pins for port 5

| | Correspondence between related register bits and pins | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Pin name** | **-** | **-** | **-** | **-** | **P53** | **P52** | **P51** | **P50** |
| PDR5 | - | - | - | - | bit3 | bit2 | bit1* | bit0* |
| DDR5 | | | | | | | | |
| PUL5 | | | | | | | | |

*: Though P50 and P51 have no pull-up function, bit0 and bit1 in the PUL5 register can still be accessed. The operation of P50 and P51 is not affected by the settings of bit0 and bit1 in the PUL5 register.

**(4) Port 5 operations**

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR5 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR5 register to external pins.
  - If data is written to the PDR5 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR5 register returns the PDR5 register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR5 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR5 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR5 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR5 register, the PDR5 register value is returned.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDR5 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR5 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR5 register, the PDR5 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR5 register corresponding to the input pin of a peripheral function to “0”.
  - Reading the PDR5 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR5 register, the PDR5 register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDR5 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR5 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PUL5 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL5 register.

## 7. Port 6

Port 6 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95810K Series Hardware Manual”.

### (1) Port 6 configuration

Port 6 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 6 data register (PDR6)
- Port 6 direction register (DDR6)
- Port 6 pull-up register (PUL6)

**(2) Block diagrams of port 6**

- P60/PPG10 pin
  This pin has the following peripheral function:
  - 8/16-bit PPG ch. 1 output pin (PPG10)

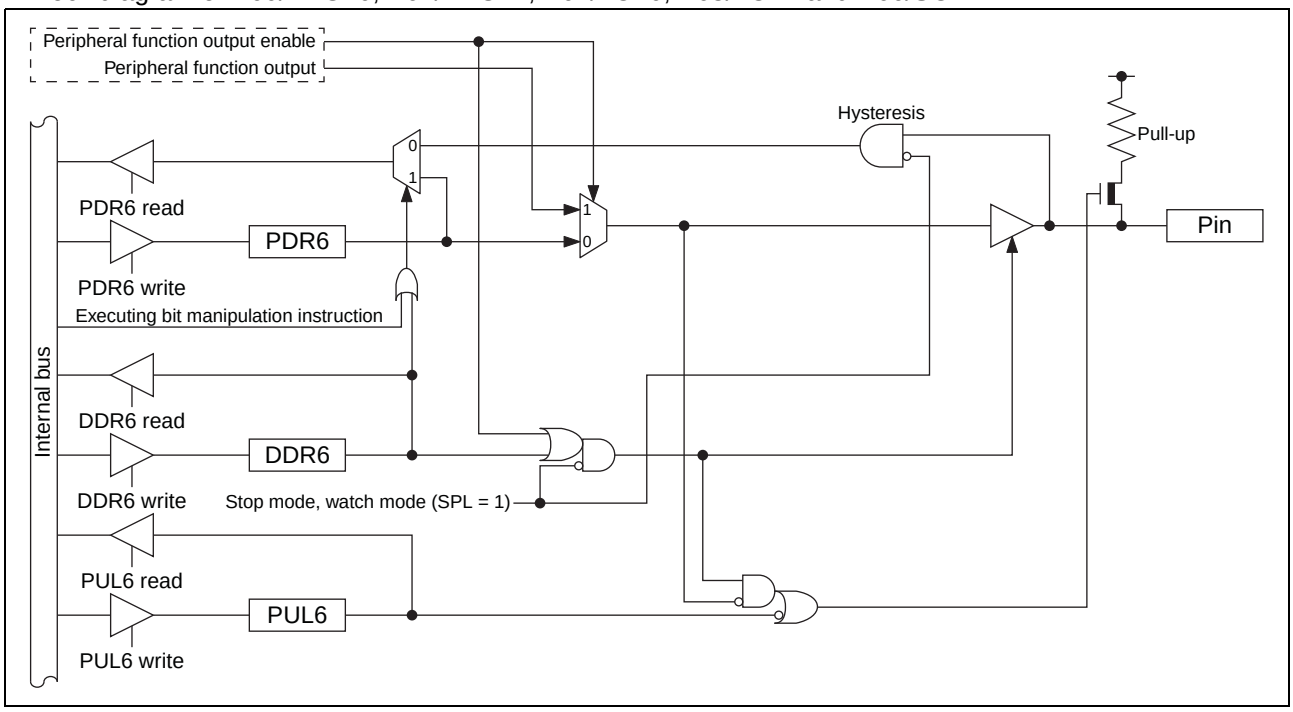
- P61/PPG11 pin
  This pin has the following peripheral function:
  - 8/16-bit PPG ch. 1 output pin (PPG11)

- P62/TO10 pin
  This pin has the following peripheral function:
  - 8/16-bit composite timer ch. 1 output pin (TO10)

- P63/TO11 pin
  This pin has the following peripheral function:
  - 8/16-bit composite timer ch. 1 output pin (TO11)

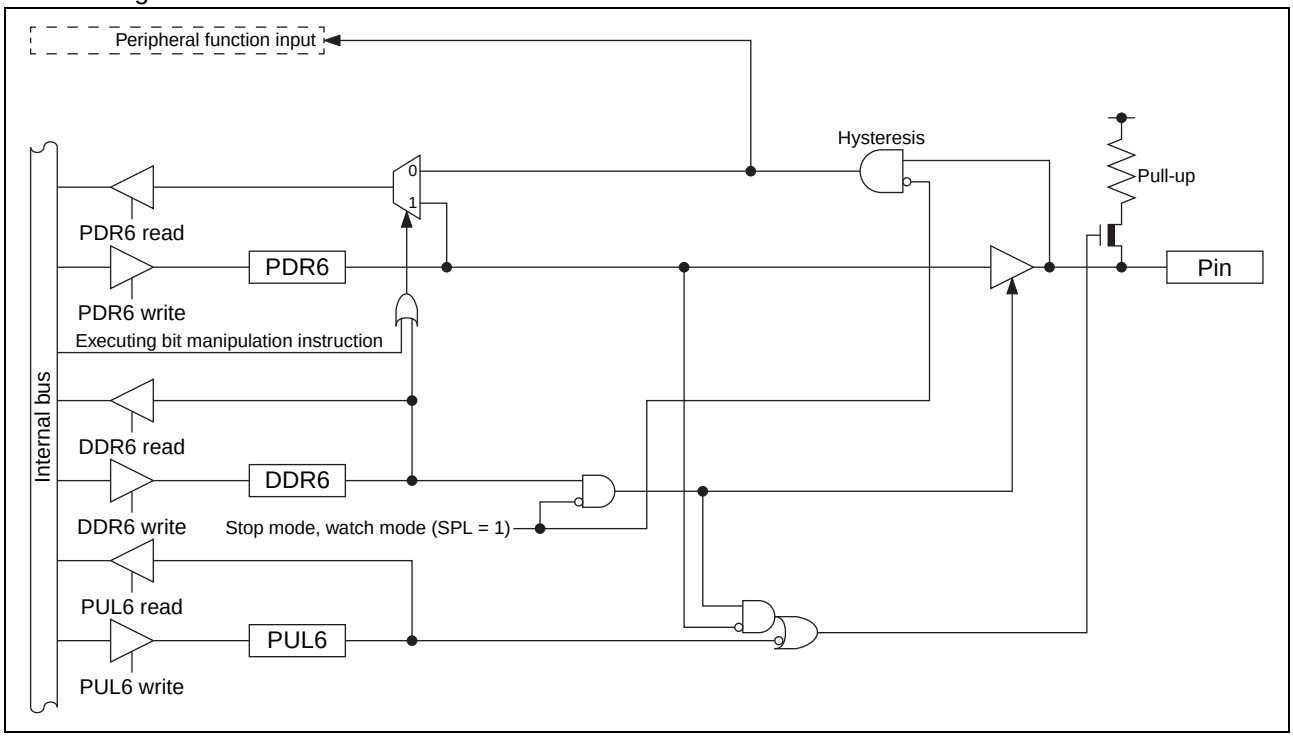
- P66/SOT pin
  This pin has the following peripheral function:
  - LIN-UART data output pin (SOT)

- Block diagram of P60/PPG10, P61/PPG11, P62/TO10, P63/TO11 and P66/SOT



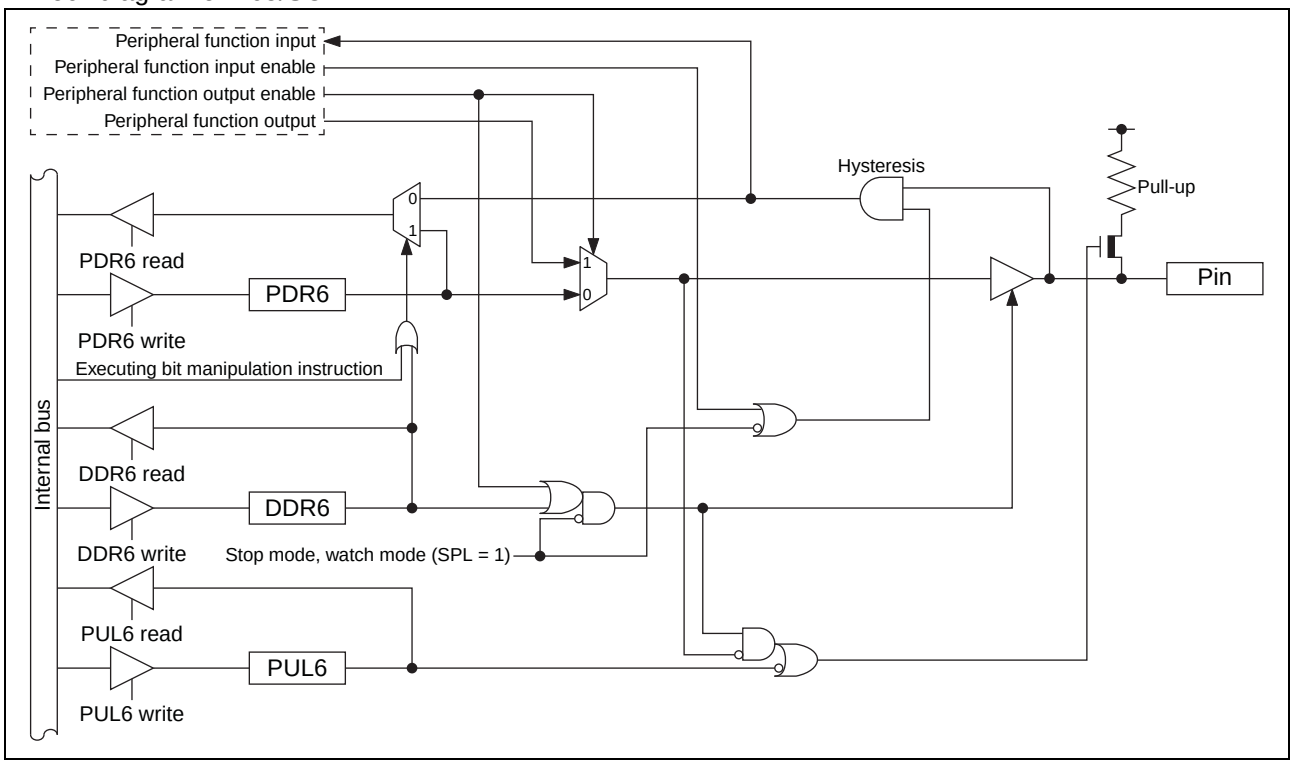
- P64/EC1 pin
  This pin has the following peripheral function:
  - 8/16-bit composite timer ch. 1 clock input pin (EC1)

- Block diagram of P64/EC1



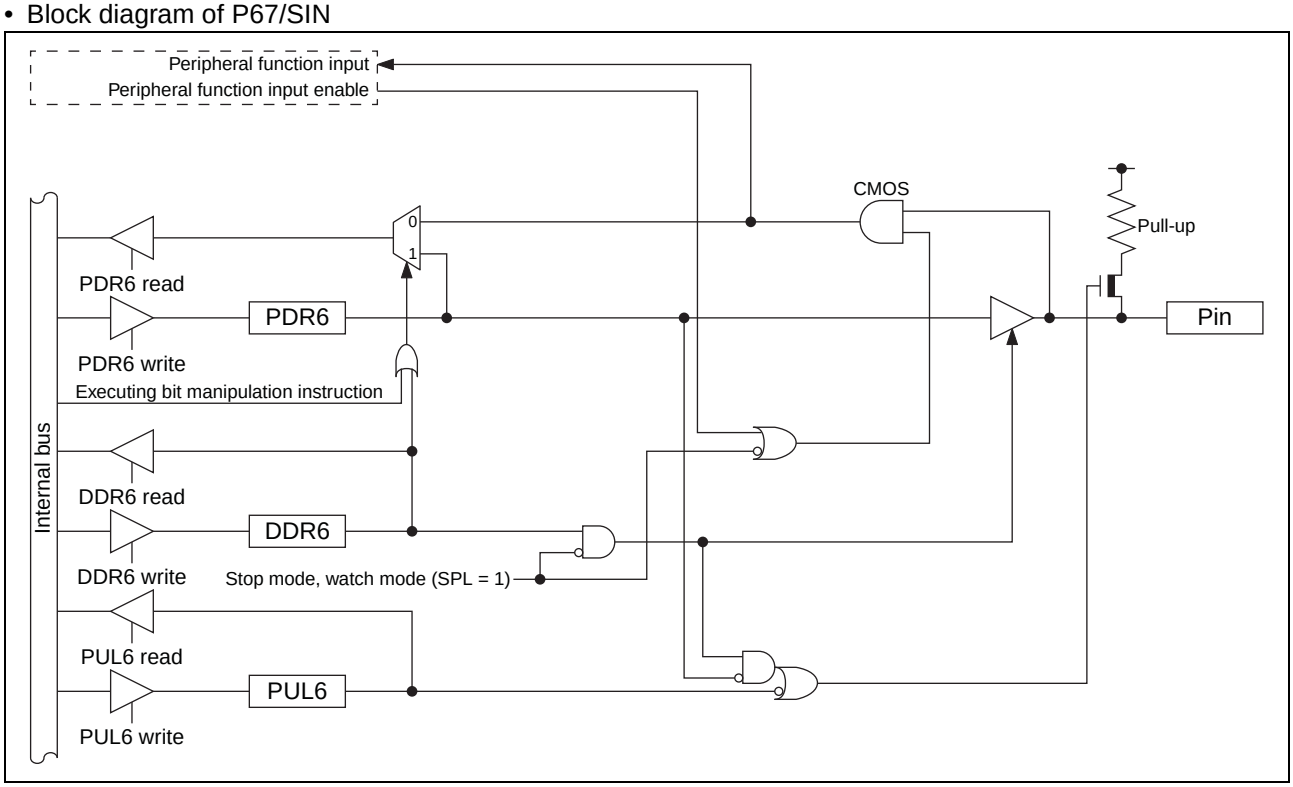

- P65/SCK pin
  This pin has the following peripheral function:
  - LIN-UART clock I/O pin (SCK)

- Block diagram of P65/SCK



- P67/SIN pin
  This pin has the following peripheral function:
  - LIN-UART data input pin (SIN)

- Block diagram of P67/SIN



### (3) Port 6 registers

• Port 6 register functions

| Register abbreviation | Data | Read | Read by read-modify-write (RMW) instruction | Write |
|---|---|---|---|---|
| PDR6 | 0 | Pin state is “L” level. | PDR6 value is “0”. | As output port, outputs “L” level. |
| | 1 | Pin state is “H” level. | PDR6 value is “1”. | As output port, outputs “H” level. |
| DDR6 | 0 | Port input enabled | | |
| | 1 | Port output enabled | | |
| PUL6 | 0 | Pull-up disabled | | |
| | 1 | Pull-up enabled | | |

• Correspondence between registers and pins for port 6

| | Correspondence between related register bits and pins | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Pin name** | **P67** | **P66** | **P65** | **P64** | **P63** | **P62** | **P61** | **P60** |
| PDR6 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| DDR6 | | | | | | | | |
| PUL6 | | | | | | | | |

**(4) Port 6 operations**

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR6 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR6 register to external pins.
  - If data is written to the PDR6 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR6 register returns the PDR6 register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR6 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR6 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR6 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDR6 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR6 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR6 register corresponding to the input pin of a peripheral function to “0”.
  - Reading the PDR6 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDR6 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR6 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input of P65/SCK and P67/SIN is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PUL6 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL6 register.

## 8. Port 7

Port 7 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95810K Series Hardware Manual”.

### (1) Port 7 configuration

Port 7 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 7 data register (PDR7)
- Port 7 direction register (DDR7)
- Port 7 pull-up register (PUL7)

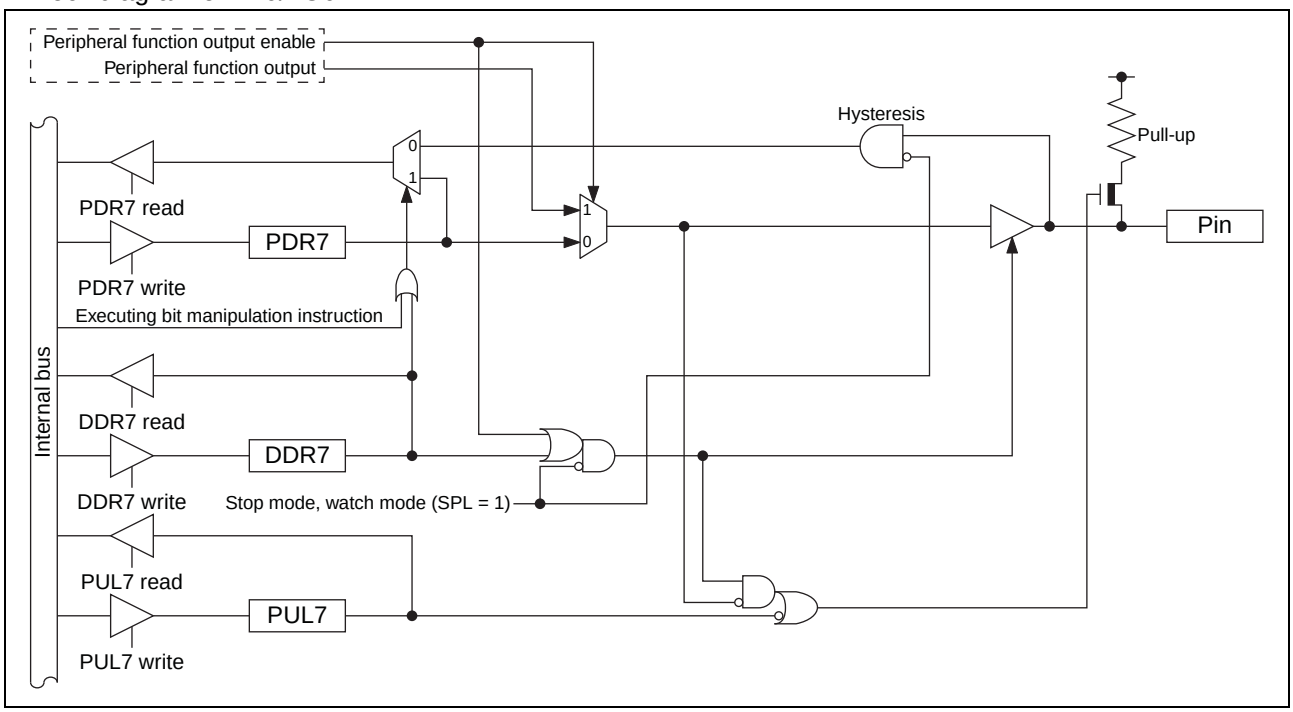
### (2) Block diagrams of port 7

- P70/TO0 pin

  This pin has the following peripheral function:

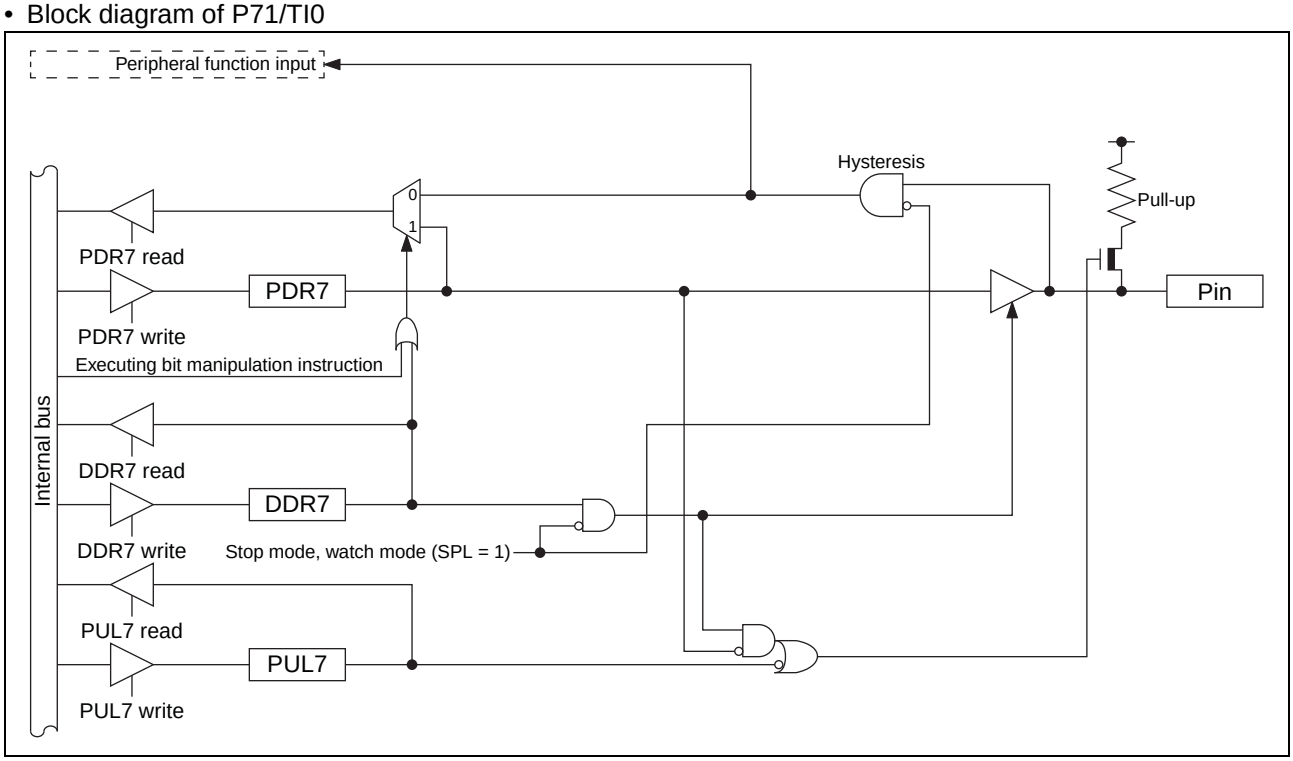
  - 16-bit reload timer ch. 0 output pin (TO0)

- Block diagram of P70/TO0



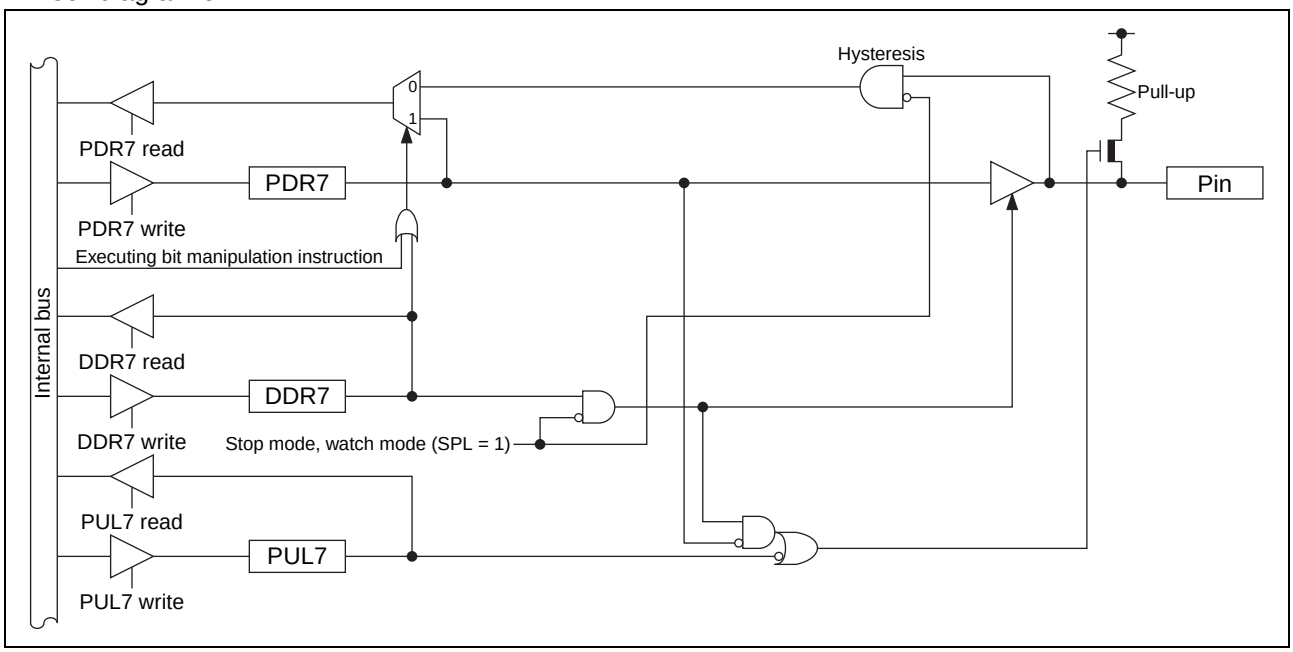
- P71/TI0 pin
  This pin has the following peripheral function:
  - 16-bit reload timer ch. 0 input pin (TI0)

- Block diagram of P71/TI0




- P72 pin

- Block diagram of P72



### (3) Port 7 registers

• Port 7 register functions

| Register abbreviation | Data | Read | Read by read-modify-write (RMW) instruction | Write |
|---|---|---|---|---|
| PDR7 | 0 | Pin state is “L” level. | PDR7 value is “0”. | As output port, outputs “L” level. |
| | 1 | Pin state is “H” level. | PDR7 value is “1”. | As output port, outputs “H” level. |
| DDR7 | 0 | Port input enabled | | |
| | 1 | Port output enabled | | |
| PUL7 | 0 | Pull-up disabled | | |
| | 1 | Pull-up enabled | | |

• Correspondence between registers and pins for port 7

| | Correspondence between related register bits and pins | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Pin name** | **-** | **-** | **-** | **-** | **-** | **P72** | **P71** | **P70** |
| PDR7 | - | - | - | - | - | bit2 | bit1 | bit0 |
| DDR7 | | | | | | | | |
| PUL7 | | | | | | | | |

**(4) Port 7 operations**

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR7 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR7 register to external pins.
  - If data is written to the PDR7 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR7 register returns the PDR7 register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR7 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR7 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR7 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR7 register, the PDR7 register value is returned.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDR7 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR7 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR7 register, the PDR7 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR7 register corresponding to the input pin of a peripheral function to “0”.
  - Reading the PDR7 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR7 register, the PDR7 register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDR7 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR7 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PUL7 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL7 register.

## 9. Port 8

Port 8 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95810K Series Hardware Manual”.

### (1) Port 8 configuration

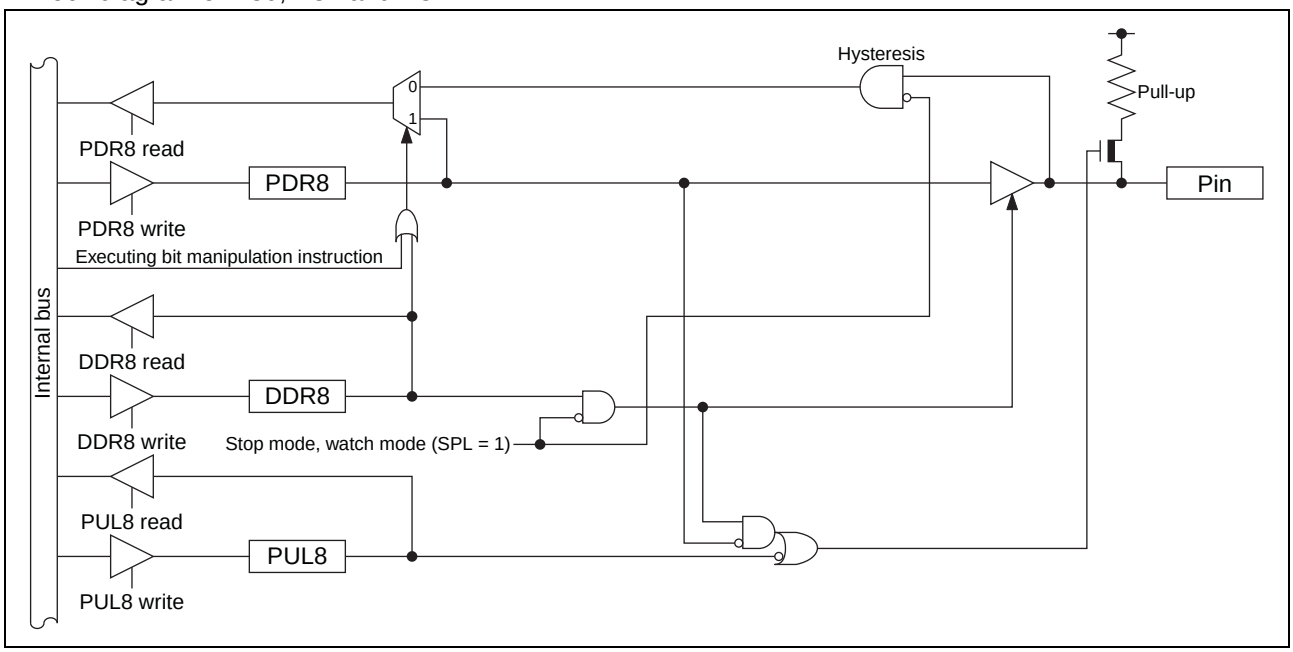
Port 8 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 8 data register (PDR8)
- Port 8 direction register (DDR8)
- Port 8 pull-up register (PUL8)

### (2) Block diagrams of port 8

- P80 pin
- P81 pin
- P82 pin

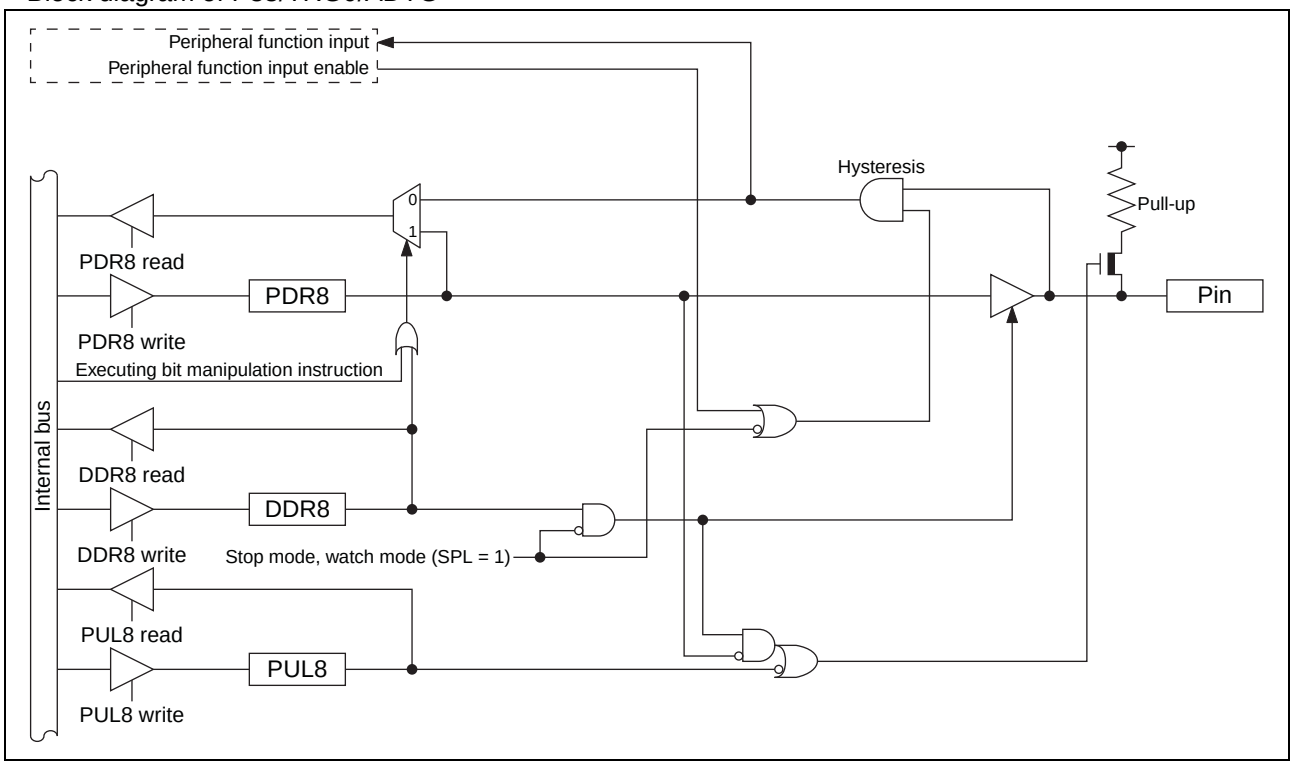
- Block diagram of P80, P81 and P82



- P83/TRG0/ADTG* pin
  This pin has the following peripheral function:
  - 16-bit PPG timer ch. 0 trigger input pin (TRG0)
  - 8/10-bit A/D converter trigger input pin (ADTG)

*: TRG0 and ADTG can be mapped to either P13 or P83 by using the SYSC register.

- Block diagram of P83/TRG0/ADTG



### (3) Port 8 registers

• Port 8 register functions

| Register abbreviation | Data | Read | Read by read-modify-write (RMW) instruction | Write |
|---|---|---|---|---|
| PDR8 | 0 | Pin state is “L” level. | PDR8 value is “0”. | As output port, outputs “L” level. |
| | 1 | Pin state is “H” level. | PDR8 value is “1”. | As output port, outputs “H” level. |
| DDR8 | 0 | Port input enabled | | |
| | 1 | Port output enabled | | |
| PUL8 | 0 | Pull-up disabled | | |
| | 1 | Pull-up enabled | | |

• Correspondence between registers and pins for port 8

| | Correspondence between related register bits and pins | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Pin name** | **-** | **-** | **-** | **-** | **P83** | **P82** | **P81** | **P80** |
| PDR8 | - | - | - | - | bit3 | bit2 | bit1 | bit0 |
| DDR8 | | | | | | | | |
| PUL8 | | | | | | | | |

**(4) Port 8 operations**

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR8 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR8 register to external pins.
  - If data is written to the PDR8 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR8 register returns the PDR8 register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR8 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR8 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR8 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR8 register, the PDR8 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR8 register corresponding to the input pin of a peripheral function to “0”.
  - Reading the PDR8 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR8 register, the PDR8 register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDR8 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR8 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input of P83/TRG0/ADTG is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PUL8 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL8 register.

## 10. Port E

Port E is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95810K Series Hardware Manual”.

### (1) Port E configuration

Port E is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port E data register (PDRE)
- Port E direction register (DDRE)
- Port E pull-up register (PULE)

### (2) Block diagrams of port E

- PE0/INT10 pin

  This pin has the following peripheral function:
  - External interrupt input pin (INT10)

- PE1/INT11 pin

  This pin has the following peripheral function:
  - External interrupt input pin (INT11)

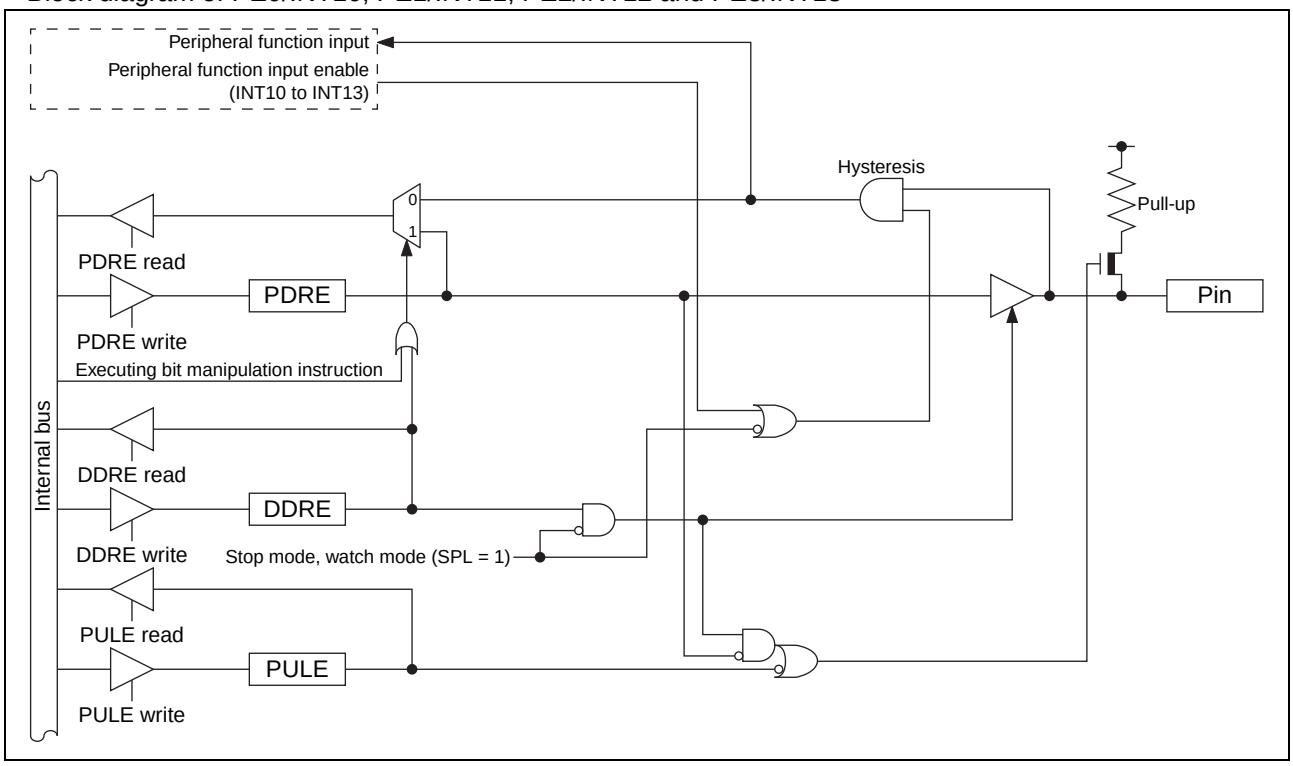
- PE2/INT12 pin

  This pin has the following peripheral function:
  External interrupt input pin (INT12)

- PE3/INT13 pin

  This pin has the following peripheral function:
  - External interrupt input pin (INT13)

- Block diagram of PE0/INT10, PE1/INT11, PE2/INT12 and PE3/INT13



### (3) Port E registers

• Port E register functions

| Register abbreviation | Data | Read | Read by read-modify-write (RMW) instruction | Write |
|---|---|---|---|---|
| PDRE | 0 | Pin state is “L” level. | PDRE value is “0”. | As output port, outputs “L” level. |
| | 1 | Pin state is “H” level. | PDRE value is “1”. | As output port, outputs “H” level. |
| DDRE | 0 | Port input enabled | | |
| | 1 | Port output enabled | | |
| PULE | 0 | Pull-up disabled | | |
| | 1 | Pull-up enabled | | |

• Correspondence between registers and pins for port E

| | Correspondence between related register bits and pins | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Pin name** | **-** | **-** | **-** | **-** | **PE3** | **PE2** | **PE1** | **PE0** |
| PDRE | - | - | - | - | bit3 | bit2 | bit1 | bit0 |
| DDRE | | | | | | | | |
| PULE | | | | | | | | |

**(4) Port E operations**

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRE register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRE register to external pins.
  - If data is written to the PDRE register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRE register returns the PDRE register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRE register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRE register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRE register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRE register, the PDRE register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDRE register corresponding to the input pin of a peripheral function to “0”.
  - Reading the PDRE register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDRE register, the PDRE register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDRE register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRE register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input is enabled for the external interrupt (INT10 to INT13), the input is enabled and not blocked.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation as an external interrupt input pin
  - Set the bit in the DDRE register corresponding to the external interrupt input pin to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - The pin value is always input to the external interrupt circuit. When using a pin for a function other than the interrupt, disable the external interrupt function corresponding to that pin.

- Operation of the pull-up register
  Setting the bit in the PULE register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PULE register.

## 11. Port F

Port F is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95810K Series Hardware Manual”.

### (1) Port F configuration

Port F is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port F data register (PDRF)
- Port F direction register (DDRF)

### (2) Block diagrams of port F

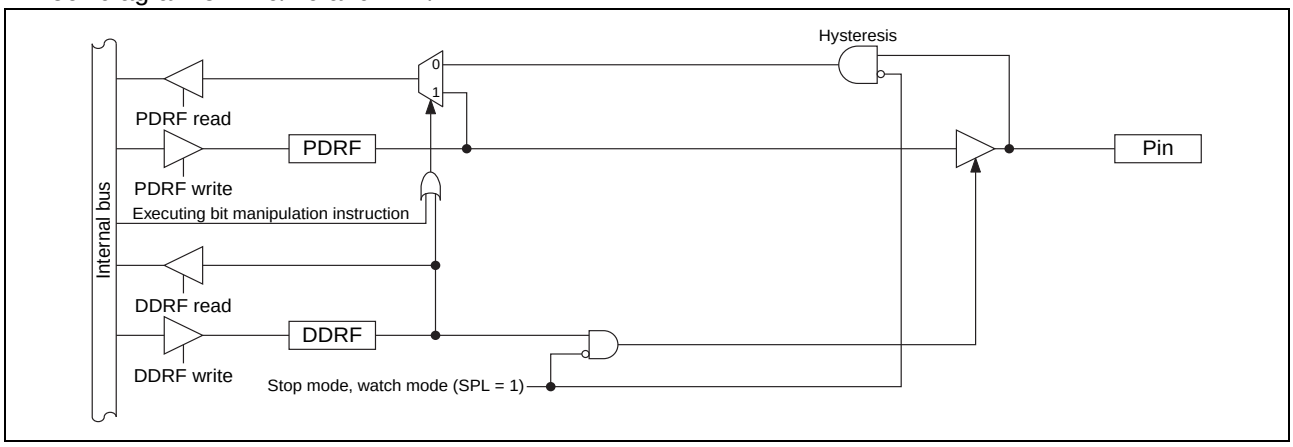
- PF0/X0 pin

  This pin has the following peripheral function:
  - Main clock input oscillation pin (X0)

- PF1/X1 pin

  This pin has the following peripheral function:
  - Main clock I/O oscillation pin (X1)

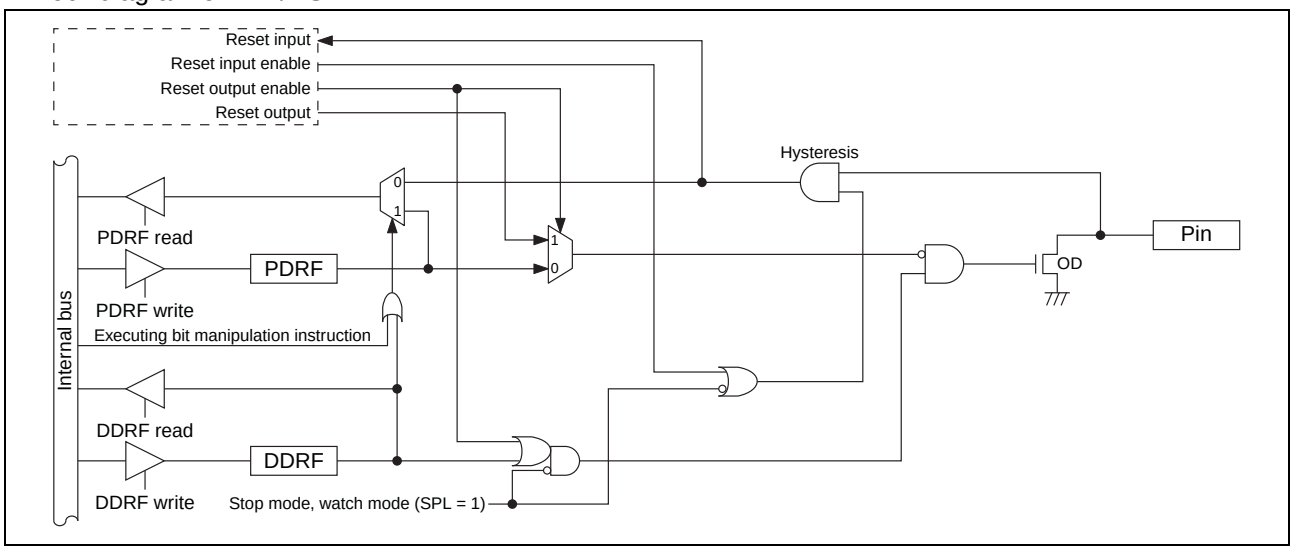
- Block diagram of PF0/X0 and PF1/X1




- PF2/$\overline{\text{RST}}$ pin

  This pin has the following peripheral function:
  - Reset pin ($\overline{\text{RST}}$)

- Block diagram of PF2/$\overline{\text{RST}}$



### (3) Port F registers

• Port F register functions

| Register abbreviation | Data | Read | Read by read-modify-write (RMW) instruction | Write |
|---|---|---|---|---|
| PDRF | 0 | Pin state is “L” level. | PDRF value is “0”. | As output port, outputs “L” level. |
| | 1 | Pin state is “H” level. | PDRF value is “1”. | As output port, outputs “H” level.* |
| DDRF | 0 | Port input enabled | | |
| | 1 | Port output enabled | | |

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

• Correspondence between registers and pins for port F

| | Correspondence between related register bits and pins | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Pin name** | **-** | **-** | **-** | **-** | **-** | **PF2** | **PF1** | **PF0** |
| PDRF | - | - | - | - | - | bit2* | bit1 | bit0 |
| DDRF | | | | | | | | |

*: When the external reset is selected (SYSC:RSTEN = 1), the port function cannot be used.

### (4) Port F operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRF register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRF register to external pins.
  - If data is written to the PDRF register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRF register returns the PDRF register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRF register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRF register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRF register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRF register, the PDRF register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDRF register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRF register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

## 12. Port G

Port G is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95810K Series Hardware Manual”.

### (1) Port G configuration

Port G is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port G data register (PDRG)
- Port G direction register (DDRG)
- Port G pull-up register (PULG)

### (2) Block diagram of port G

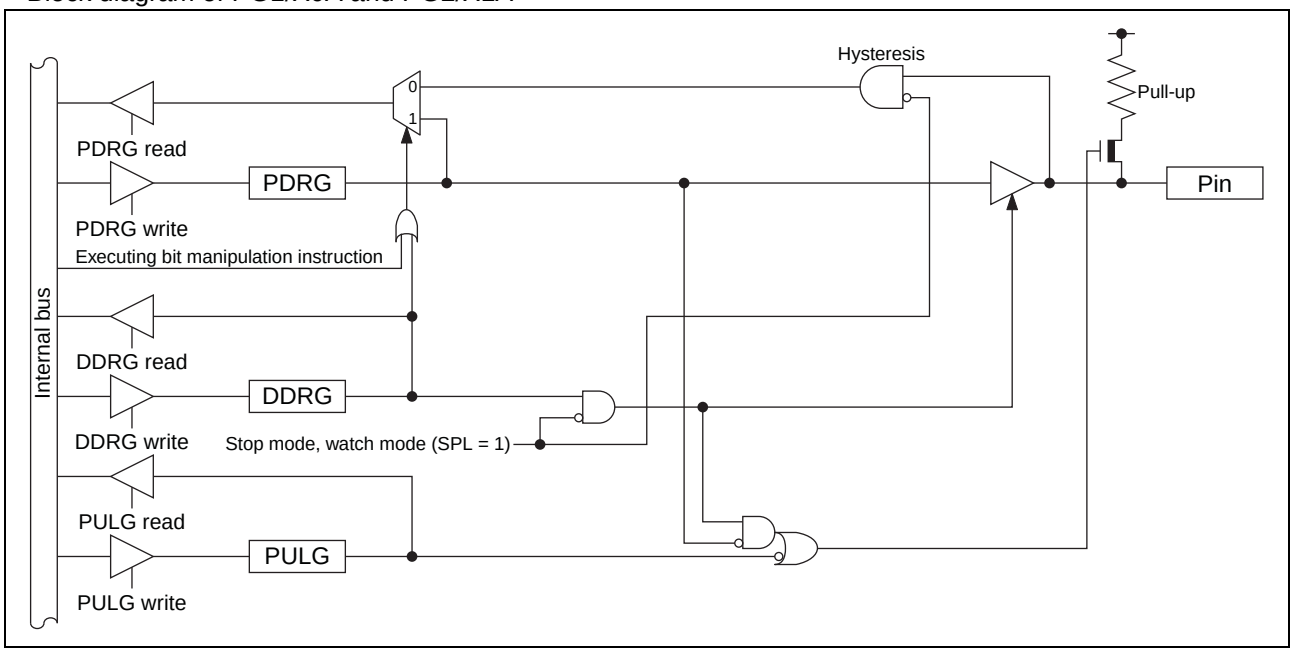
- PG1/X0A pin

  This pin has the following peripheral function:
  - Subclock input oscillation pin (X0A)

- PG2/X1A pin

  This pin has the following peripheral function:
  - Subclock I/O oscillation pin (X1A)

- Block diagram of PG1/X0A and PG2/X1A



### (3) Port G registers

• Port G register functions

| Register abbreviation | Data | Read | Read by read-modify-write (RMW) instruction | Write |
|---|---|---|---|---|
| PDRG | 0 | Pin state is “L” level. | PDRG value is “0”. | As output port, outputs “L” level. |
| | 1 | Pin state is “H” level. | PDRG value is “1”. | As output port, outputs “H” level. |
| DDRG | 0 | Port input enabled | | |
| | 1 | Port output enabled | | |
| PULG | 0 | Pull-up disabled | | |
| | 1 | Pull-up enabled | | |

• Correspondence between registers and pins for port G

| | Correspondence between related register bits and pins | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Pin name** | **-** | **-** | **-** | **-** | **-** | **PG2** | **PG1** | **-** |
| PDRG | - | - | - | - | - | bit2 | bit1 | - |
| DDRG | | | | | | | | |
| PULG | | | | | | | | |

**(4) Port G operations**

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRG register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRG register to external pins.
  - If data is written to the PDRG register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRG register returns the PDRG register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRG register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRG register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRG register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRG register, the PDRG register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDRG register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRG register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PULG register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PULG register.

## ■ INTERRUPT SOURCE TABLE

| Interrupt source | Interrupt request number | Vector table address | | Interrupt level setting register | | Priority order of interrupt sources of the same level (occurring simultaneously) |
|---|---|---|---|---|---|---|
| | | Upper | Lower | Register | Bit | |
| External interrupt ch. 0 | IRQ00 | 0xFFFA | 0xFFFB | ILR0 | L00 [1:0] | High ↑ |
| External interrupt ch. 4 | | | | | | |
| External interrupt ch. 1 | IRQ01 | 0xFFF8 | 0xFFF9 | ILR0 | L01 [1:0] | |
| External interrupt ch. 5 | | | | | | |
| External interrupt ch. 2 | IRQ02 | 0xFFF6 | 0xFFF7 | ILR0 | L02 [1:0] | |
| External interrupt ch. 6 | | | | | | |
| External interrupt ch. 3 | IRQ03 | 0xFFF4 | 0xFFF5 | ILR0 | L03 [1:0] | |
| External interrupt ch. 7 | | | | | | |
| Comparator ch. 1 | | | | | | |
| UART/SIO ch. 0 | IRQ04 | 0xFFF2 | 0xFFF3 | ILR1 | L04 [1:0] | |
| 8/16-bit composite timer ch. 0 (lower) | IRQ05 | 0xFFF0 | 0xFFF1 | ILR1 | L05 [1:0] | |
| 8/16-bit composite timer ch. 0 (upper) | IRQ06 | 0xFFEE | 0xFFEF | ILR1 | L06 [1:0] | |
| LIN-UART (reception) | IRQ07 | 0xFFEC | 0xFFED | ILR1 | L07 [1:0] | |
| LIN-UART (transmission) | IRQ08 | 0xFFEA | 0xFFEB | ILR2 | L08 [1:0] | |
| 8/16-bit PPG ch. 1 (lower) | IRQ09 | 0xFFE8 | 0xFFE9 | ILR2 | L09 [1:0] | |
| 8/16-bit PPG ch. 1 (upper) | IRQ10 | 0xFFE6 | 0xFFE7 | ILR2 | L10 [1:0] | |
| 16-bit reload timer ch. 0 | IRQ11 | 0xFFE4 | 0xFFE5 | ILR2 | L11 [1:0] | |
| 8/16-bit PPG ch. 0 (upper) | IRQ12 | 0xFFE2 | 0xFFE3 | ILR3 | L12 [1:0] | |
| 8/16-bit PPG ch. 0 (lower) | IRQ13 | 0xFFE0 | 0xFFE1 | ILR3 | L13 [1:0] | |
| 8/16-bit composite timer ch. 1 (upper) | IRQ14 | 0xFFDE | 0xFFDF | ILR3 | L14 [1:0] | |
| 16-bit PPG timer ch. 0 | IRQ15 | 0xFFDC | 0xFFDD | ILR3 | L15 [1:0] | |
| $I^2C$ bus interface ch. 0 | IRQ16 | 0xFFDA | 0xFFDB | ILR4 | L16 [1:0] | |
| 16-bit PPG timer ch. 1 | IRQ17 | 0xFFD8 | 0xFFD9 | ILR4 | L17 [1:0] | |
| 8/10-bit A/D converter | IRQ18 | 0xFFD6 | 0xFFD7 | ILR4 | L18 [1:0] | |
| Time-base timer | IRQ19 | 0xFFD4 | 0xFFD5 | ILR4 | L19 [1:0] | |
| Watch prescaler | IRQ20 | 0xFFD2 | 0xFFD3 | ILR5 | L20 [1:0] | |
| Watch counter | | | | | | |
| External interrupt ch. 10 | IRQ21 | 0xFFD0 | 0xFFD1 | ILR5 | L21 [1:0] | |
| External interrupt ch. 11 | | | | | | |
| External interrupt ch. 12 | | | | | | |
| External interrupt ch. 13 | | | | | | |
| Comparator ch. 0 | | | | | | |
| 8/16-bit composite timer ch. 1 (lower) | IRQ22 | 0xFFCE | 0xFFCF | ILR5 | L22 [1:0] | |
| Flash memory | IRQ23 | 0xFFCC | 0xFFCD | ILR5 | L23 [1:0] | Low ↓ |

## ■ PIN STATES IN EACH MODE

| Pin name | Normal operation | Sleep mode | Stop mode | | Watch mode | | On reset |
|---|---|---|---|---|---|---|---|
| | | | SPL=0 | SPL=1 | SPL=0 | SPL=1 | |
| PF0/X0 | Oscillation input | Oscillation input | Hi-Z | Hi-Z | Hi-Z | Hi-Z | — |
| | I/O port*1 | I/O port*1 | - Previous state kept<br>- Input blocked*1*2 | - Hi-Z<br>- Input blocked*1*2 | - Previous state kept<br>- Input blocked*1*2 | - Hi-Z<br>- Input blocked*1*2 | - Hi-Z<br>- Input enabled*3 (However, it does not function.) |
| PF1/X1 | Oscillation input | Oscillation input | Hi-Z | Hi-Z | Hi-Z | Hi-Z | — |
| | I/O port*1 | I/O port*1 | - Previous state kept<br>- Input blocked*1*2 | - Hi-Z<br>- Input blocked*1*2 | - Previous state kept<br>- Input blocked*1*2 | - Hi-Z<br>- Input blocked*1*2 | - Hi-Z<br>- Input enabled*3 (However, it does not function.) |
| PF2/$\overline{\text{RST}}$ | Reset input*4 | Reset input*4 | Reset input | Reset input | Reset input | Reset input | Reset input*4 |
| | I/O port | I/O port | - Previous state kept<br>- Input blocked*1*2 | - Hi-Z<br>- Input blocked*1*2 | - Previous state kept<br>- Input blocked*1*2 | - Hi-Z<br>- Input blocked*1*2 | - Hi-Z<br>- Input enabled*3 (However, it does not function.) |
| PG1/X0A | Oscillation input | Oscillation input | Hi-Z | Hi-Z | Hi-Z | Hi-Z | — |
| | I/O port*1 | I/O port*1 | - Previous state kept<br>- Input blocked*1*2 | - Hi-Z*5<br>- Input blocked*1*2 | - Previous state kept<br>- Input blocked*1*2 | - Hi-Z*5<br>- Input blocked*1*2 | - Hi-Z<br>- Input enabled*3 (However, it does not function.) |
| PG2/X1A | Oscillation input | Oscillation input | Hi-Z | Hi-Z | Hi-Z | Hi-Z | — |
| | I/O port*1 | I/O port*1 | - Previous state kept<br>- Input blocked*1*2 | - Hi-Z*5<br>- Input blocked*1*2 | - Previous state kept<br>- Input blocked*1*2 | - Hi-Z*5<br>- Input blocked*1*2 | - Hi-Z<br>- Input enabled*3 (However, it does not function.) |
| P00/INT00<br>P01/INT01<br>P02/INT02<br>P03/INT03<br>P04/INT04<br>P05/INT05<br>P06/INT06<br>P07/INT07<br>P10/UI0 | I/O port/ peripheral function I/O | I/O port/ peripheral function I/O | - Previous state kept<br>- Input blocked*2*6 | - Hi-Z*5<br>- Input blocked*2*6 | - Previous state kept<br>- Input blocked*2*6 | - Hi-Z*5<br>- Input blocked*2*6 | - Hi-Z<br>- Input enabled*3 (However, it does not function.) |
| P11/UO0 | I/O port/ peripheral function I/O | I/O port/ peripheral function I/O | - Previous state kept<br>- Input blocked*2 | - Hi-Z*5<br>- Input blocked*2 | - Previous state kept<br>- Input blocked*2 | - Hi-Z*5<br>- Input blocked*2 | - Hi-Z<br>- Input enabled*3 (However, it does not function.) |

*(Continued)*

| Pin name | Normal operation | Sleep mode | Stop mode | | Watch mode | | On reset |
|---|---|---|---|---|---|---|---|
| | | | SPL=0 | SPL=1 | SPL=0 | SPL=1 | |
| P12/DBG | I/O port/ peripheral function I/O | I/O port/ peripheral function I/O | - Previous state kept<br>- Input blocked*2 | - Hi-Z<br>- Input blocked*2 | - Previous state kept<br>- Input blocked*2 | - Hi-Z<br>- Input blocked*2 | - Hi-Z<br>- Input enabled*3 (However, it does not function.) |
| P13/UCK0/ TRG0/ADTG | I/O port/ peripheral function I/O | I/O port/ peripheral function I/O | - Previous state kept<br>- Input blocked*2, *6 | - Hi-Z*5<br>- Input blocked*2, *6 | - Previous state kept<br>- Input blocked*2, *6 | - Hi-Z*5<br>- Input blocked*2, *6 | - Hi-Z<br>- Input enabled*3 (However, it does not function.) |
| P14/PPG0<br>P20/PPG00<br>P21/PPG01<br>P22/TO00<br>P23/TO01 | I/O port/ peripheral function I/O | I/O port/ peripheral function I/O | - Previous state kept<br>- Input blocked*2 | - Hi-Z*5<br>- Input blocked*2 | - Previous state kept<br>- Input blocked*2 | - Hi-Z*5<br>- Input blocked*2 | - Hi-Z<br>- Input enabled*3 (However, it does not function.) |
| P24/EC0 | I/O port/ peripheral function I/O | I/O port/ peripheral function I/O | - Previous state kept<br>- Input blocked*2, *6 | - Hi-Z*5<br>- Input blocked*2, *6 | - Previous state kept<br>- Input blocked*2, *6 | - Hi-Z*5<br>- Input blocked*2, *6 | - Hi-Z<br>- Input enabled*3 (However, it does not function.) |
| P32/AN02/ CMP0_O<br>P35/AN05/ CMP1_O | I/O port/ peripheral function I/O/ analog input | I/O port/ peripheral function I/O/ analog input | - Previous state kept*8<br>- Input blocked*2 | - Hi-Z*5<br>- Input blocked*2 | - Previous state kept*8<br>- Input blocked*2 | - Hi-Z*5<br>- Input blocked*2 | - Hi-Z<br>- Input blocked*2 |
| P30/AN00/ CMP0_N<br>P31/AN01/ CMP0_P<br>P33/AN03/ CMP1_N<br>P34/AN04/ CMP1_P | I/O port/ peripheral function I/O/ analog input | I/O port/ peripheral function I/O/ analog input | - Previous state kept<br>- Input blocked*2, *7 | - Hi-Z*5<br>- Input blocked*2, *7 | - Previous state kept<br>- Input blocked*2, *7 | - Hi-Z*5<br>- Input blocked*2, *7 | - Hi-Z<br>- Input blocked*2 |
| P36/AN06<br>P37/AN07<br>P40/AN08<br>P41/AN09<br>P42/AN10<br>P43/AN11 | I/O port/ analog input | I/O port/ analog input | - Previous state kept<br>- Input blocked*2 | - Hi-Z*5<br>- Input blocked*2 | - Previous state kept<br>- Input blocked*2 | - Hi-Z*5<br>- Input blocked*2 | - Hi-Z<br>- Input blocked*2 |
| P50/SCL<br>P51/SDA | I/O port/ peripheral function I/O | I/O port/ peripheral function I/O | - Previous state kept<br>- Input blocked*2, *9 | - Hi-Z<br>- Input blocked*2, *9 | - Previous state kept<br>- Input blocked*2, *9 | - Hi-Z<br>- Input blocked*2, *9 | - Hi-Z<br>- Input enabled*3 (However, it does not function.) |

*(Continued)*

*(Continued)*

| Pin name | Normal operation | Sleep mode | Stop mode | | Watch mode | | On reset |
|---|---|---|---|---|---|---|---|
| | | | SPL=0 | SPL=1 | SPL=0 | SPL=1 | |
| P52/PPG1<br>P53/TRG1<br>P60/PPG10<br>P61/PPG11<br>P62/TO10<br>P63/TO11<br>P64/EC1<br>P66/SOT | I/O port/ peripheral function I/O | I/O port/ peripheral function I/O | - Previous state kept<br>- Input blocked*2 | - Hi-Z*5<br>- Input blocked*2 | - Previous state kept<br>- Input blocked*2 | - Hi-Z*5<br>- Input blocked*2 | - Hi-Z<br>- Input enabled*3 (However, it does not function.) |
| P65/SCK<br>P67/SIN | I/O port/ peripheral function I/O | I/O port/ peripheral function I/O | - Previous state kept<br>- Input blocked*2, *6 | - Hi-Z*5<br>- Input blocked*2, *6 | - Previous state kept<br>- Input blocked*2, *6 | - Hi-Z*5<br>- Input blocked*2, *6 | - Hi-Z<br>- Input enabled*3 (However, it does not function.) |
| P70/TO0<br>P71/TI0 | I/O port/ peripheral function I/O | I/O port/ peripheral function I/O | - Previous state kept<br>- Input blocked*2 | - Hi-Z*5<br>- Input blocked*2 | - Previous state kept<br>- Input blocked*2 | - Hi-Z*5<br>- Input blocked*2 | - Hi-Z<br>- Input enabled*3 (However, it does not function.) |
| P72<br>P80<br>P81<br>P82 | I/O port | I/O port | - Previous state kept<br>- Input blocked*2 | - Hi-Z*5<br>- Input blocked*2 | - Previous state kept<br>- Input blocked*2 | - Hi-Z*5<br>- Input blocked*2 | - Hi-Z<br>- Input enabled*3 (However, it does not function.) |
| P83/TRG0/ ADTG<br>PE0/INT10<br>PE1/INT11<br>PE2/INT12<br>PE3/INT13 | I/O port/ peripheral function I/O | I/O port/ peripheral function I/O | - Previous state kept<br>- Input blocked*2, *6 | - Hi-Z*5<br>- Input blocked*2, *6 | - Previous state kept<br>- Input blocked*2, *6 | - Hi-Z*5<br>- Input blocked*2, *6 | - Hi-Z<br>- Input enabled*3 (However, it does not function.) |

SPL: Pin state setting bit in the standby control register (STBC:SPL)
Hi-Z: High impedance
*1: The pin stays at the state shown when configured as a general-purpose I/O port.
*2: “Input blocked” means direct input gate operation from the pin is disabled.
*3: “Input enabled” means that the input function is enabled. While the input function is enabled, a pull-up or pull-down operation has to be performed in order to prevent leaks due to external input. If a pin is used as an output port, its pin state is the same as that of other ports.
*4: The PF2/$\overline{\text{RST}}$ pin stays at the state shown when configured as a reset pin.
*5: The pull-up control setting is still effective.
*6: Though input is blocked, an external interrupt can be input when the external interrupt request is enabled.
*7: Though input is blocked, an analog signal can also be input to generate a comparator interrupt when the comparator interrupt is enabled.
*8: The output function of the comparator is still in operation in stop mode and watch mode.
*9: The $I^2C$ bus interface can wake up the MCU in stop mode or watch mode when its MCU standby mode wake-up function is enabled. For details of the MCU standby mode wakeup function, refer to “CHAPTER 24 $I^2C$ BUS INTERFACE” in “New 8FX MB95810K Series Hardware Manual”.

## ■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage*1 | $AV_{CC}$, $V_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6 | V | *2 |
| | AVR | $V_{SS}$ – 0.3 | $V_{SS}$ + 6 | V | |
| Input voltage*1 | $V_I$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6 | V | *3 |
| Output voltage*1 | $V_O$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6 | V | *3 |
| Maximum clamp current | $I_{CLAMP}$ | –2 | +2 | mA | Applicable to specific pins*4 |
| Total maximum clamp current | $\Sigma\lvert I_{CLAMP}\rvert$ | — | 20 | mA | Applicable to specific pins*4 |
| “L” level maximum output current | $I_{OL}$ | — | 15 | mA | |
| “L” level average current | $I_{OLAV1}$ | — | 4 | mA | Other than P00 to P07<br>Average output current =<br>operating current × operating ratio (1 pin) |
| | $I_{OLAV2}$ | | 12 | | P00 to P07<br>Average output current =<br>operating current × operating ratio (1 pin) |
| “L” level total maximum output current | $\Sigma I_{OL}$ | — | 100 | mA | |
| “L” level total average output current | $\Sigma I_{OLAV}$ | — | 37 | mA | Total average output current =<br>operating current × operating ratio<br>(Total number of pins) |
| “H” level maximum output current | $I_{OH}$ | — | –15 | mA | |
| “H” level average current | $I_{OHAV1}$ | — | –4 | mA | Other than P00 to P07<br>Average output current =<br>operating current × operating ratio (1 pin) |
| | $I_{OHAV2}$ | | –8 | | P00 to P07<br>Average output current =<br>operating current × operating ratio (1 pin) |
| “H” level total maximum output current | $\Sigma I_{OH}$ | — | –100 | mA | |
| “H” level total average output current | $\Sigma I_{OHAV}$ | — | –47 | mA | Total average output current =<br>operating current × operating ratio<br>(Total number of pins) |
| Power consumption | $P_d$ | — | 320 | mW | |
| Operating temperature | $T_A$ | –40 | +85 | °C | |
| Storage temperature | $T_{stg}$ | –55 | +150 | °C | |

*(Continued)*

*(Continued)*

*1: These parameters are based on the condition that $V_{SS}$ is 0.0 V.

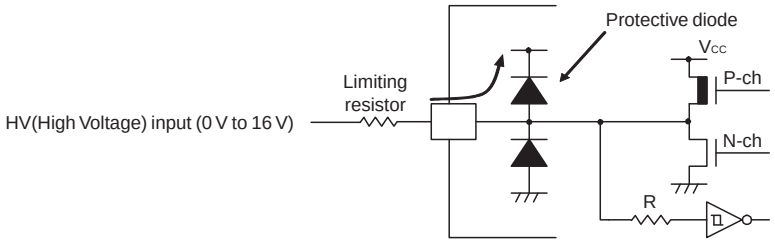
*2: Apply equal potential to $AV_{CC}$ and $V_{CC}$. AVR must not exceed $AV_{CC}$.

*3: $V_1$ and $V_0$ must not exceed $V_{CC}$ + 0.3 V. $V_1$ must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the $I_{CLAMP}$ rating is used instead of the $V_I$ rating.

*4: Specific pins: P00 to P07, P10, P11, P13, P14, P20 to P24, P30 to P37, P40 to P43, P52, P53, P60 to P67, P70 to P72, P80 to P83, PE0 to PE3, PF0, PF1, PG1, PG2

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the $V_{CC}$ voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the $V_{CC}$ pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit:

- Input/Output equivalent circuit




WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.
Do not exceed any of these ratings.

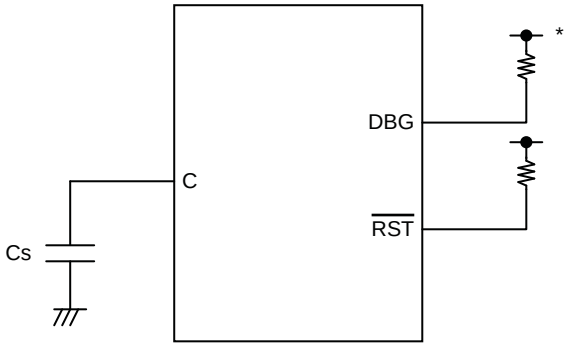
## 2. Recommended Operating Conditions

($V_{SS}$ = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage | $AV_{CC}$, $V_{CC}$ | 2.88 | 5.5 | V | |
| A/D converter reference input voltage | AVR | $AV_{CC}$ – 0.1 | $AV_{CC}$ | V | |
| Decoupling capacitor | $C_S$ | 0.022 | 1 | µF | * |
| Operating temperature | $T_A$ | –40 | +85 | °C | Other than on-chip debug mode |
| | | +5 | +35 | | On-chip debug mode |

*: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the $V_{CC}$ pin must have a capacitance equal to or larger than the capacitance of $C_S$. For the connection to a decoupling capacitor $C_S$, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and $C_S$ and the distance between $C_S$ and the $V_{SS}$ pin when designing the layout of a printed circuit board.

- DBG / $\overline{RST}$ / C pins connection diagram




*: Connect the DBG pin to an external pull-up resistor of 2 kΩ or above. After power-on, ensure that the DBG pin does not stay at “L” level until the reset output is released. The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

### 3. DC Characteristics

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level input voltage | $V_{IHI}$ | P10, P50, P51, P67 | — | 0.7 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | CMOS input level |
| | $V_{IHS}$ | Other than P10, P50, P51, P67, PF2 | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | Hysteresis input |
| | $V_{IHM}$ | PF2 | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | Hysteresis input |
| "L" level input voltage | $V_{ILI}$ | P10, P50, P51, P67 | — | $V_{SS}$ – 0.3 | — | 0.3 $V_{CC}$ | V | CMOS input level |
| | $V_{ILS}$ | Other than P10, P50, P51, P67, PF2 | — | $V_{SS}$ – 0.3 | — | 0.2 $V_{CC}$ | V | Hysteresis input |
| | $V_{ILM}$ | PF2 | — | $V_{SS}$ – 0.3 | — | 0.2 $V_{CC}$ | V | Hysteresis input |
| Open-drain output application voltage | $V_D$ | P12, P50, P51, PF2 | — | $V_{SS}$ – 0.3 | — | $V_{SS}$ + 5.5 | V | |
| "H" level output voltage | $V_{OH1}$ | Output pins other than P00 to P07, P12, PF2 | $I_{OH}$ = –4 mA | $V_{CC}$ – 0.5 | — | — | V | |
| | $V_{OH2}$ | P00 to P07 | $I_{OH}$ = –8 mA | $V_{CC}$ – 0.5 | — | — | V | |
| "L" level output voltage | $V_{OL1}$ | Output pins other than P00 to P07 | $I_{OL}$ = 4 mA | — | — | 0.4 | V | |
| | $V_{OL2}$ | P00 to P07 | $I_{OL}$ = 12 mA | — | — | 0.4 | V | |
| Input leak current (Hi-Z output leak current) | $I_{LI}$ | All input pins | 0.0 V < $V_I$ < $V_{CC}$ | –5 | — | +5 | µA | When the internal pull-up resistor is disabled |
| Internal pull-up resistor | $R_{PULL}$ | Other than P12, P50, P51, PF0 to PF2 | $V_I$ = 0 V | 25 | 50 | 100 | kΩ | When the internal pull-up resistor is enabled |
| Input capacitance | $C_{IN}$ | Other than $AV_{CC}$, $AV_{SS}$, AVR, $V_{CC}$ and $V_{SS}$ | f = 1 MHz | — | 5 | 15 | pF | |

*(Continued)*

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ*1 | Max*2 | | |
| Power supply current*3 | $I_{CC}$ | $V_{CC}$ (External clock operation) | $F_{CH}$ = 32 MHz<br>$F_{MP}$ = 16 MHz<br>Main clock mode<br>(divided by 2) | — | 4.8 | 5.8 | mA | Except during Flash memory programming and erasing |
| | | | | — | 10.1 | 13.8 | mA | During Flash memory programming and erasing |
| | $I_{CCS}$ | | $F_{CH}$ = 32 MHz<br>$F_{MP}$ = 16 MHz<br>Main sleep mode<br>(divided by 2) | — | 1.9 | 3 | mA | |
| | $I_{CCL}$ | | $F_{CL}$ = 32 kHz<br>$F_{MPL}$ = 16 kHz<br>Subclock mode<br>(divided by 2)<br>$T_A$ = +25 °C | — | 65.9 | 145 | µA | |
| | $I_{CCLS}$ | | $F_{CL}$ = 32 kHz<br>$F_{MPL}$ = 16 kHz<br>Subsleep mode<br>(divided by 2)<br>$T_A$ = +25 °C | — | 11.2 | 16 | µA | In deep standby mode |
| | $I_{CCT}$ | | $F_{CL}$ = 32 kHz<br>Watch mode<br>Main stop mode<br>$T_A$ = +25 °C | — | 8.6 | 13 | µA | In deep standby mode |
| | $I_{CCMPLL}$ | $V_{CC}$ | $F_{MCRPLL}$ = 16 MHz<br>$F_{MP}$ = 16 MHz<br>Main CR PLL clock mode<br>(multiplied by 4)<br>$T_A$ = +25 °C | — | 5.1 | 6.8 | mA | |
| | $I_{CCMCR}$ | | $F_{CRH}$ = 4 MHz<br>$F_{MP}$ = 4 MHz<br>Main CR clock mode | — | 1.4 | 4.6 | mA | |
| | $I_{CCSCR}$ | | Sub-CR clock mode<br>(divided by 2)<br>$T_A$ = +25 °C | — | 63.1 | 230 | µA | |
| | $I_{CCTS}$ | $V_{CC}$ (External clock operation) | $F_{CH}$ = 32 MHz<br>Time-base timer mode<br>$T_A$ = +25 °C | — | 360 | 455 | µA | In deep standby mode |
| | $I_{CCH}$ | | Substop mode<br>$T_A$ = +25 °C | — | 8.8 | 13 | µA | In deep standby mode |

*(Continued)*

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ*1 | Max*2 | | |
| Power supply current*3 | $I_V$ | $V_{CC}$ | Current consumption of the comparator | — | 60 | 160 | µA | |
| | $I_{LVD}$ | | Current consumption of the low-voltage detection reset circuit | — | 4 | 7 | µA | With the LVD reset already enabled by the LVD reset circuit control register (LVDCC) |
| | $I_{CRH}$ | | Current consumption of the main CR oscillator | — | 240 | 320 | µA | |
| | $I_{CRL}$ | | Current consumption of the sub-CR oscillator oscillating at 100 kHz | — | 7 | 20 | µA | |
| | $I_{NSTBY}$ | | Current consumption difference between normal standby mode and deep standby mode $T_A$ = +25 °C | — | 22 | 30 | µA | |
| | $I_A$ | $AV_{CC}$ | $V_{CC}$ = 5.5 V $F_{CH}$ = 16 MHz Current consumption of the A/D converter | — | 2 | 3.1 | mA | |
| | $I_{AH}$ | | $F_{CRH}$ = 4 MHz $F_{MP}$ = 4 MHz Current consumption with the A/D converter halted $T_A$ = +25 °C | — | 1 | 5 | µA | |

*1: $V_{CC}$ = 5.0 V, $T_A$ = +25 °C

*2: $V_{CC}$ = 5.5 V, $T_A$ = +85 °C (unless otherwise specified)

*(Continued)*

*(Continued)*

*3:
- The power supply current is determined by the external clock. When the low-voltage detection reset circuit is selected, the power supply current is the sum of adding the current consumption of the low-voltage detection reset circuit ($I_{LVD}$) to one of the values from $I_{CC}$ to $I_{CCH}$. In addition, when both the low-voltage detection reset circuit and a CR oscillator are selected, the power supply current is the sum of adding up the current consumption of the low-voltage detection reset circuit ($I_{LVD}$), the current consumption of the CR oscillators ($I_{CRH}$ or $I_{CRL}$) and one of the values from $I_{CC}$ to $I_{CCH}$. In on-chip debug mode, the main CR oscillator ($I_{CRH}$) and the low-voltage detection reset circuit are always in operation, and current consumption therefore increases accordingly.
- See “4. AC Characteristics (1) Clock Timing” for $F_{CH}$, $F_{CL}$, $F_{CRH}$ and $F_{MCRPLL}$.
- See “4. AC Characteristics (2) Source Clock/Machine Clock” for $F_{MP}$ and $F_{MPL}$.
- The power supply current value in standby mode is measured in deep standby mode. The current consumption in normal standby mode is higher than that in deep standby mode. The power supply current value in normal standby mode can be found by adding the current consumption difference between normal standby mode and deep standby mode ($I_{NSTBY}$) to the power supply current value in deep standby mode. For details of normal standby mode and deep standby mode, refer to “CHAPTER 3 CLOCK CONTROLLER” in “New 8FX MB95810K Series Hardware Manual”.

## 4. AC Characteristics

### (1) Clock Timing

($V_{CC}$ = 2.88 V to 5.5 V, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Clock frequency | $F_{CH}$ | X0, X1 | — | 1 | — | 16.25 | MHz | When the main oscillation circuit is used |
| | | X0 | X1: open | 1 | — | 12 | MHz | When the main external clock is used |
| | | X0, X1 | * | 1 | — | 32.5 | MHz | |
| | $F_{CRH}$ | — | — | 3.92 | 4 | 4.08 | MHz | Operating conditions<br>• The main CR clock is used.<br>• 0 °C ≤ $T_A$ ≤ +70 °C |
| | | | | 3.8 | 4 | 4.2 | MHz | Operating conditions<br>• The main CR clock is used.<br>• – 40 °C ≤ $T_A$ < 0 °C,<br>+ 70 °C < $T_A$ ≤ + 85 °C |
| | $F_{MCRPLL}$ | — | — | 7.84 | 8 | 8.16 | MHz | Operating conditions<br>• PLL multiplication rate: 2<br>• 0 °C ≤ $T_A$ ≤ +70 °C |
| | | | | 7.6 | 8 | 8.4 | MHz | Operating conditions<br>• PLL multiplication rate: 2<br>• – 40 °C ≤ $T_A$ < 0 °C,<br>+ 70 °C < $T_A$ ≤ + 85 °C |
| | | | | 9.8 | 10 | 10.2 | MHz | Operating conditions<br>• PLL multiplication rate: 2.5<br>• 0 °C ≤ $T_A$ ≤ +70 °C |
| | | | | 9.5 | 10 | 10.5 | MHz | Operating conditions<br>• PLL multiplication rate: 2.5<br>• – 40 °C ≤ $T_A$ < 0 °C,<br>+ 70 °C < $T_A$ ≤ + 85 °C |
| | | | | 11.76 | 12 | 12.24 | MHz | Operating conditions<br>• PLL multiplication rate: 3<br>• 0 °C ≤ $T_A$ ≤ +70 °C |
| | | | | 11.4 | 12 | 12.6 | MHz | Operating conditions<br>• PLL multiplication rate: 3<br>• – 40 °C ≤ $T_A$ < 0 °C,<br>+ 70 °C < $T_A$ ≤ + 85 °C |
| | | | | 15.68 | 16 | 16.32 | MHz | Operating conditions<br>• PLL multiplication rate: 4<br>• 0 °C ≤ $T_A$ ≤ +70 °C |
| | | | | 15.2 | 16 | 16.8 | MHz | Operating conditions<br>• PLL multiplication rate: 4<br>• – 40 °C ≤ $T_A$ < 0 °C,<br>+ 70 °C < $T_A$ ≤ + 85 °C |
| | $F_{CL}$ | X0A, X1A | — | — | 32.768 | — | kHz | When the suboscillation circuit is used |
| | | | | — | 32.768 | — | kHz | When the sub-external clock is used |
| | $F_{CRL}$ | — | — | 50 | 100 | 150 | kHz | When the sub-CR clock is used |

*(Continued)*

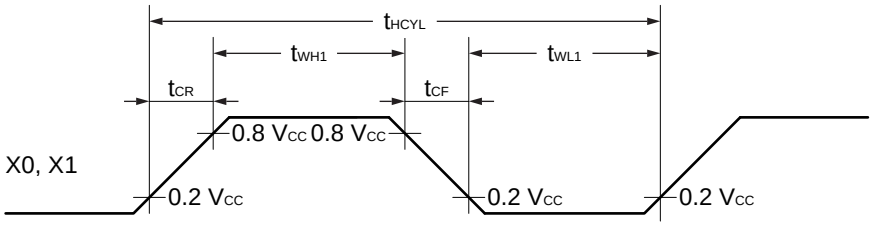
*(Continued)*

($V_{CC}$ = 2.88 V to 5.5 V, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Clock cycle time | $t_{HCYL}$ | X0, X1 | — | 61.5 | — | 1000 | ns | When the main oscillation circuit is used |
| | | X0 | X1: open | 83.4 | — | 1000 | ns | When an external clock is used |
| | | X0, X1 | * | 30.8 | — | 1000 | ns | |
| | $t_{LCYL}$ | X0A, X1A | — | — | 30.5 | — | µs | When the subclock is used |
| Input clock pulse width | $t_{WH1}$, $t_{WL1}$ | X0 | X1: open | 33.4 | — | — | ns | When an external clock is used, the duty ratio should range between 40% and 60%. |
| | | X0, X1 | * | 12.4 | — | — | ns | |
| | $t_{WH2}$, $t_{WL2}$ | X0A | — | — | 15.2 | — | µs | |
| Input clock rising time and falling time | $t_{CR}$, $t_{CF}$ | X0, X0A | X1: open | — | — | 5 | ns | When an external clock is used |
| | | X0, X1, X0A, X1A | * | — | — | 5 | ns | |
| CR oscillation start time | $t_{CRHWK}$ | — | — | — | — | 50 | µs | When the main CR clock is used |
| | $t_{CRLWK}$ | — | — | — | — | 30 | µs | When the sub-CR clock is used |
| PLL oscillation start time | $t_{MCRPLLWK}$ | — | — | — | — | 100 | µs | When the main CR PLL clock is used |

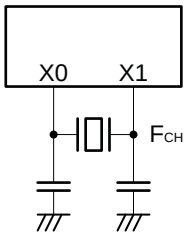
*: The external clock signal is input to X0 and the inverted external clock signal to X1.

- Input waveform generated when an external clock (main clock) is used

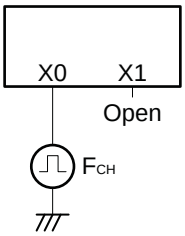



- Figure of main clock input port external connection

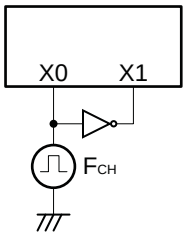
When a crystal oscillator or a ceramic oscillator is used



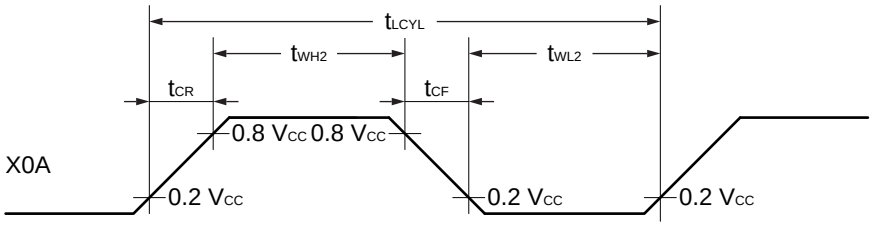

When an external clock is used (X1 is open)




When an external clock is used

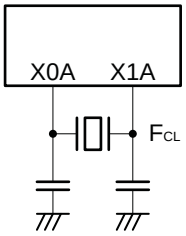



- Input waveform generated when an external clock (subclock) is used

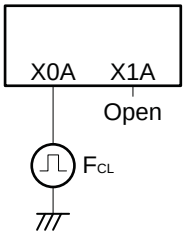



- Figure of subclock input port external connection

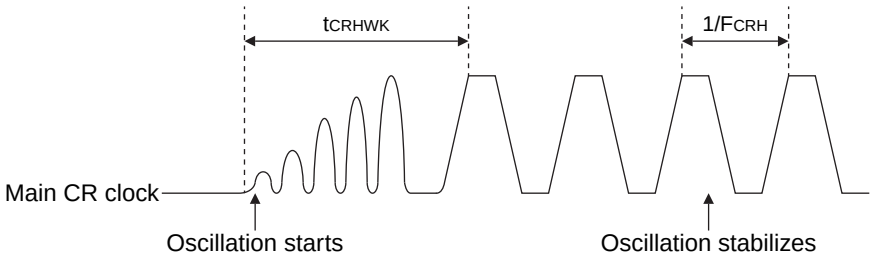
When a crystal oscillator or a ceramic oscillator is used



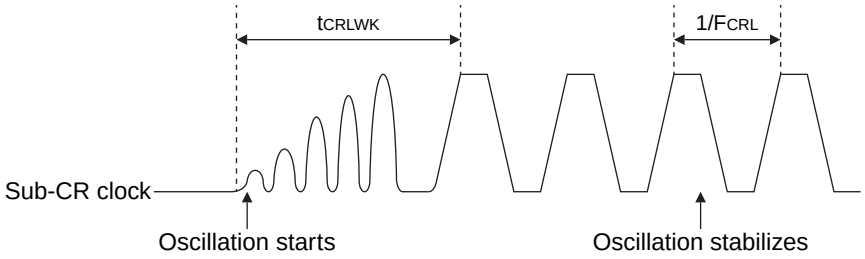

When an external clock is used



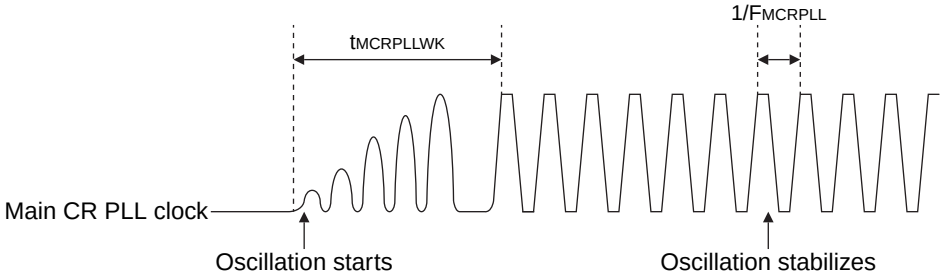

- Input waveform generated when an internal clock (main CR clock) is used



- Input waveform generated when an internal clock (sub-CR clock) is used




- Input waveform generated when an internal clock (main CR PLL clock) is used



### (2) Source Clock/Machine Clock

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Source clock cycle time*1 | $t_{SCLK}$ | — | 61.5 | — | 2000 | ns | When the main external clock is used<br>Min: $F_{CH}$ = 32.5 MHz, divided by 2<br>Max: $F_{CH}$ = 1 MHz, divided by 2 |
| | | | 62.5 | — | 1000 | ns | When the main CR clock is used<br>Min: $F_{CRH}$ = 4 MHz, multiplied by 4<br>Max: $F_{CRH}$ = 4 MHz, divided by 4 |
| | | | — | 61 | — | µs | When the suboscillation clock is used<br>$F_{CL}$ = 32.768 kHz, divided by 2 |
| | | | — | 20 | — | µs | When the sub-CR clock is used<br>$F_{CRL}$ = 100 kHz, divided by 2 |
| Source clock frequency | $F_{SP}$ | — | 0.5 | — | 16.25 | MHz | When the main oscillation clock is used |
| | | | — | 4 | 12.5 | MHz | When the main CR clock is used |
| | $F_{SPL}$ | | — | 16.384 | — | kHz | When the suboscillation clock is used |
| | | | — | 50 | — | kHz | When the sub-CR clock is used<br>$F_{CRL}$ = 100 kHz, divided by 2 |
| Machine clock cycle time*2 (minimum instruction execution time) | $t_{MCLK}$ | — | 61.5 | — | 32000 | ns | When the main oscillation clock is used<br>Min: $F_{SP}$ = 16.25 MHz, no division<br>Max: $F_{SP}$ = 0.5 MHz, divided by 16 |
| | | | 250 | — | 4000 | ns | When the main CR clock is used<br>Min: $F_{SP}$ = 4 MHz, no division<br>Max: $F_{SP}$ = 4 MHz, divided by 16 |
| | | | 61 | — | 976.5 | µs | When the suboscillation clock is used<br>Min: $F_{SPL}$ = 16.384 kHz, no division<br>Max: $F_{SPL}$ = 16.384 kHz, divided by 16 |
| | | | 20 | — | 320 | µs | When the sub-CR clock is used<br>Min: $F_{SPL}$ = 50 kHz, no division<br>Max: $F_{SPL}$ = 50 kHz, divided by 16 |
| Machine clock frequency | $F_{MP}$ | — | 0.031 | — | 16.25 | MHz | When the main oscillation clock is used |
| | | | 0.25 | — | 16 | MHz | When the main CR clock is used |
| | $F_{MPL}$ | | 1.024 | — | 16.384 | kHz | When the suboscillation clock is used |
| | | | 3.125 | — | 50 | kHz | When the sub-CR clock is used<br>$F_{CRL}$ = 100 kHz |

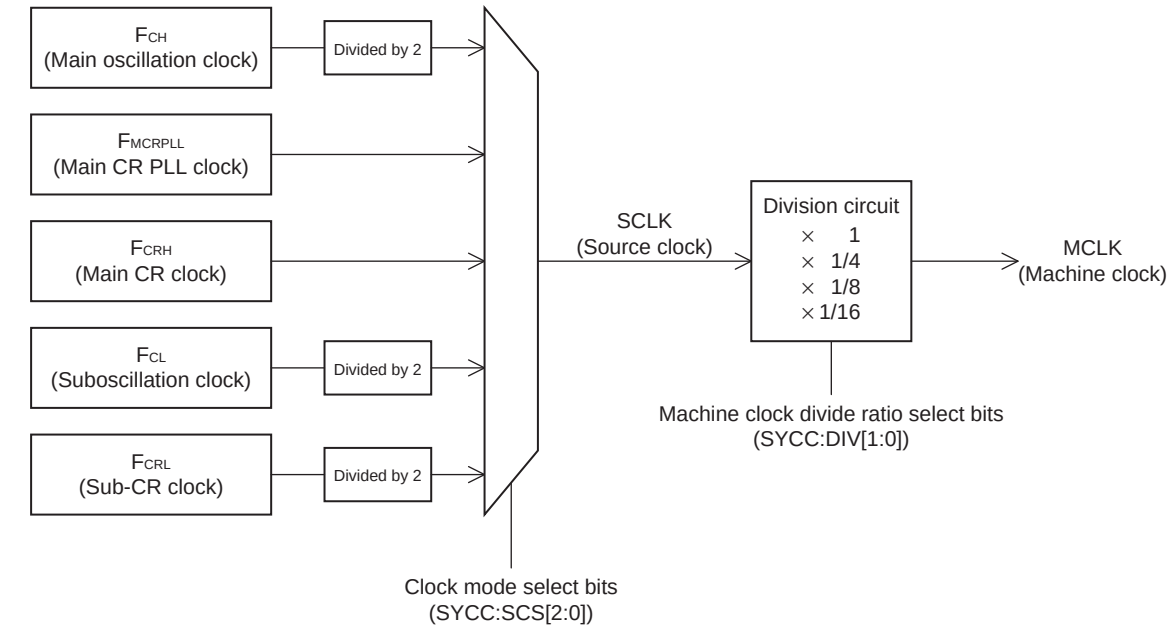
*1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- Main CR clock
- PLL multiplication of main CR clock (Select a multiplication rate from 2, 2.5, 3 and 4.)
- Subclock divided by 2
- Sub-CR clock divided by 2

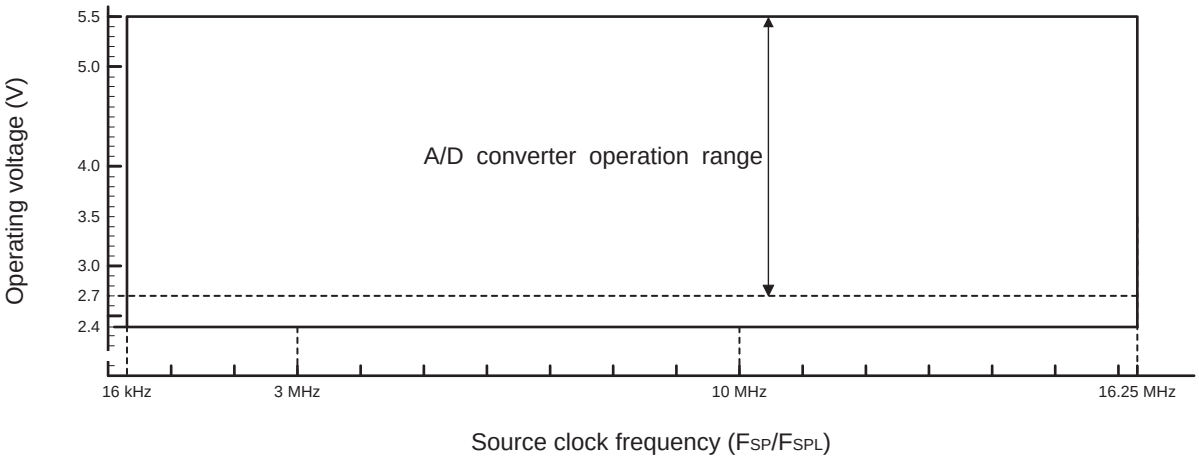
*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

- Schematic diagram of the clock generation block




- Operating voltage - Operating Frequency ($T_A$ = –40 °C to +85 °C)

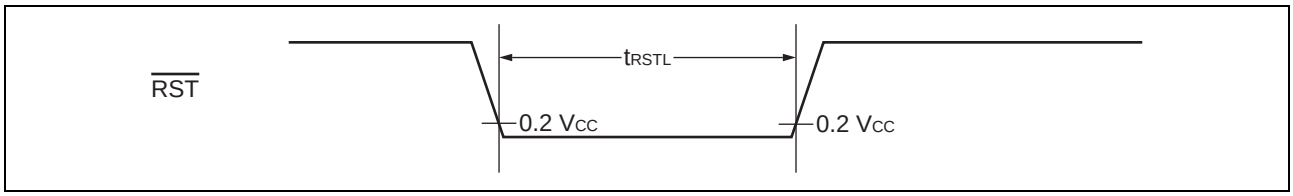


### (3) External Reset

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $\overline{RST}$ “L” level pulse width | $t_{RSTL}$ | 2 $t_{MCLK}$* | — | ns | |

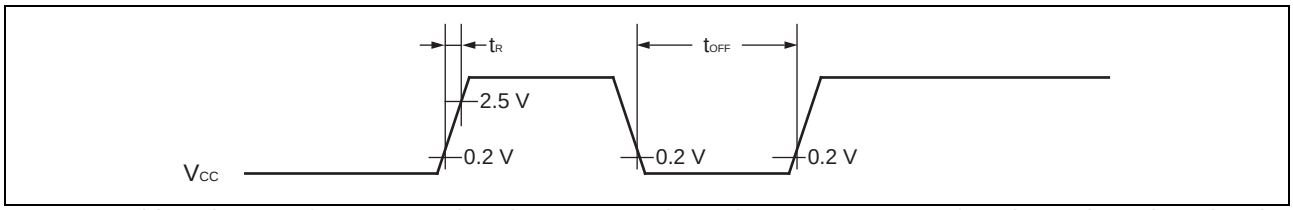
*: See “(2) Source Clock/Machine Clock” for $t_{MCLK}$.



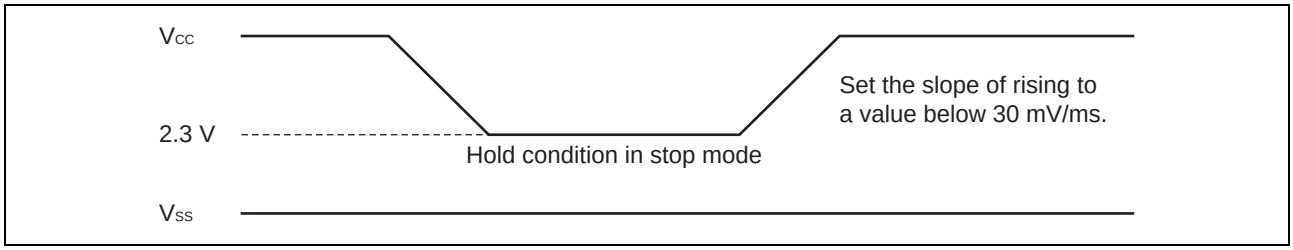
### (4) Power-on Reset

($V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Power supply rising time | $t_R$ | — | — | 50 | ms | |
| Power supply cutoff time | $t_{OFF}$ | — | 1 | — | ms | Wait time until power-on |



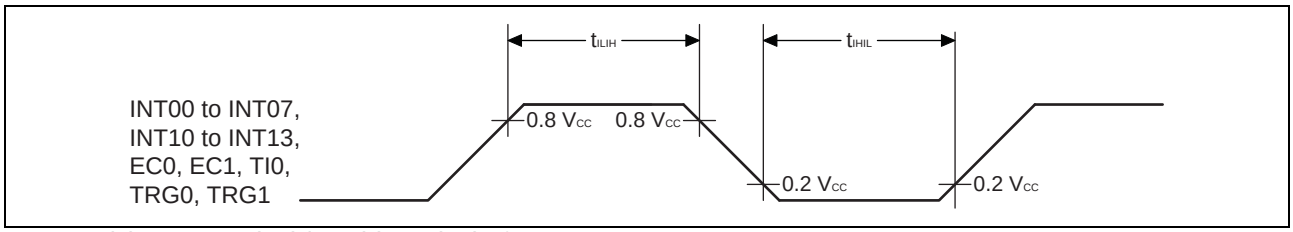

Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.



### (5) Peripheral Input Timing

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Pin name | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Peripheral input “H” pulse width | $t_{ILIH}$ | INT00 to INT07, INT10 to INT13, EC0, EC1, TI0, TRG0, TRG1 | 2 $t_{MCLK}$* | — | ns |
| Peripheral input “L” pulse width | $t_{IHIL}$ | | 2 $t_{MCLK}$* | — | ns |




*: See “(2) Source Clock/Machine Clock” for $t_{MCLK}$.

### (6) LIN-UART Timing

**Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is disabled*2. (ESCR register : SCES bit = 0, ECCR register : SCDE bit = 0)**

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

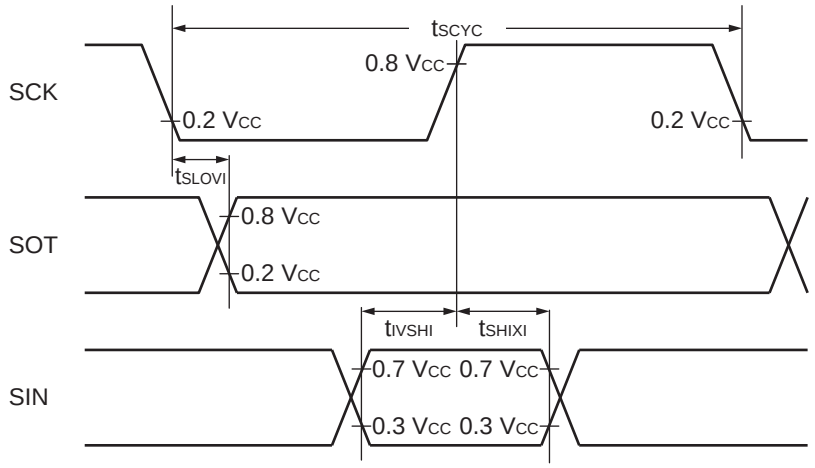
| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK | Internal clock operation output pin: $C_L$ = 80 pF + 1 TTL | 5 $t_{MCLK}$*3 | — | ns |
| SCK↓ → SOT delay time | $t_{SLOVI}$ | SCK, SOT | | –50 | +50 | ns |
| Valid SIN → SCK↑ | $t_{IVSHI}$ | SCK, SIN | | $t_{MCLK}$*3 + 80 | — | ns |
| SCK↑ → valid SIN hold time | $t_{SHIXI}$ | SCK, SIN | | 0 | — | ns |
| Serial clock “L” pulse width | $t_{SLSH}$ | SCK | External clock operation output pin: $C_L$ = 80 pF + 1 TTL | 3 $t_{MCLK}$*3–$t_R$ | — | ns |
| Serial clock “H” pulse width | $t_{SHSL}$ | SCK | | $t_{MCLK}$*3 + 10 | — | ns |
| SCK↓ → SOT delay time | $t_{SLOVE}$ | SCK, SOT | | — | 2 $t_{MCLK}$*3 + 60 | ns |
| Valid SIN → SCK↑ | $t_{IVSHE}$ | SCK, SIN | | 30 | — | ns |
| SCK↑ → valid SIN hold time | $t_{SHIXE}$ | SCK, SIN | | $t_{MCLK}$*3 + 30 | — | ns |
| SCK fall time | $t_F$ | SCK | | — | 10 | ns |
| SCK rise time | $t_R$ | SCK | | — | 10 | ns |

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

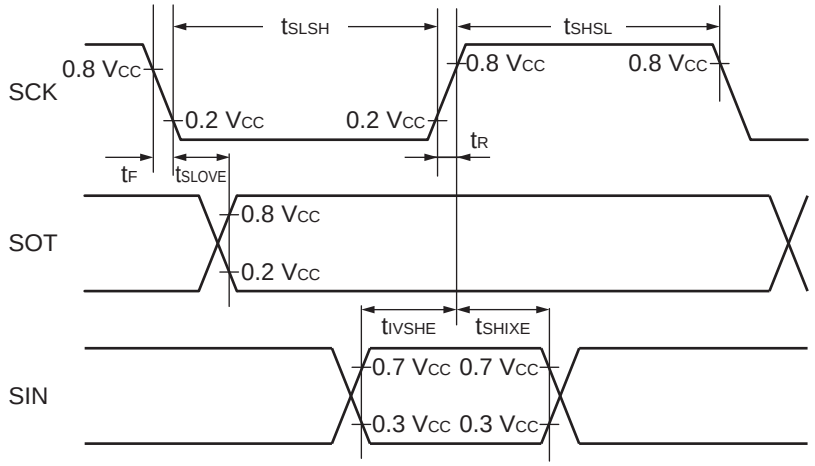
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “(2) Source Clock/Machine Clock” for $t_{MCLK}$.

- Internal shift clock mode




- External shift clock mode



**Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is disabled*2. (ESCR register : SCES bit = 1, ECCR register : SCDE bit = 0)**

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

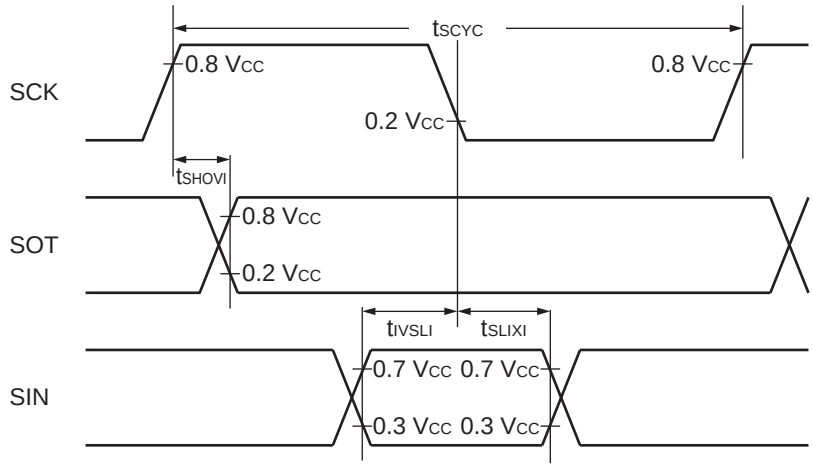
| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK | Internal clock operation output pin: $C_L$ = 80 pF + 1 TTL | 5 $t_{MCLK}$*3 | — | ns |
| SCK↑ → SOT delay time | $t_{SHOVI}$ | SCK, SOT | | –50 | +50 | ns |
| Valid SIN → SCK↓ | $t_{IVSLI}$ | SCK, SIN | | $t_{MCLK}$*3 + 80 | — | ns |
| SCK↓→ valid SIN hold time | $t_{SLIXI}$ | SCK, SIN | | 0 | — | ns |
| Serial clock “H” pulse width | $t_{SHSL}$ | SCK | External clock operation output pin: $C_L$ = 80 pF + 1 TTL | 3 $t_{MCLK}$*3 – $t_R$ | — | ns |
| Serial clock “L” pulse width | $t_{SLSH}$ | SCK | | $t_{MCLK}$*3 + 10 | — | ns |
| SCK↑ → SOT delay time | $t_{SHOVE}$ | SCK, SOT | | — | 2 $t_{MCLK}$*3 + 60 | ns |
| Valid SIN → SCK↓ | $t_{IVSLE}$ | SCK, SIN | | 30 | — | ns |
| SCK↓→ valid SIN hold time | $t_{SLIXE}$ | SCK, SIN | | $t_{MCLK}$*3 + 30 | — | ns |
| SCK fall time | $t_F$ | SCK | | — | 10 | ns |
| SCK rise time | $t_R$ | SCK | | — | 10 | ns |

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

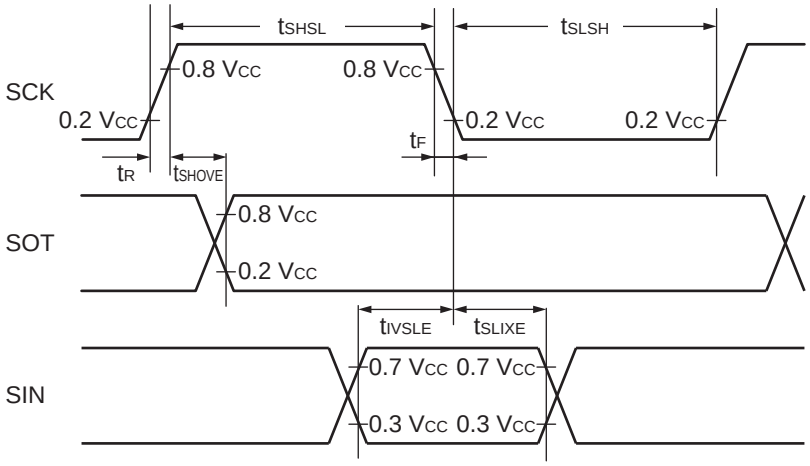
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “(2) Source Clock/Machine Clock” for $t_{MCLK}$.

- Internal shift clock mode




- External shift clock mode



**Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is enabled*2. (ESCR register : SCES bit = 0, ECCR register : SCDE bit = 1)**

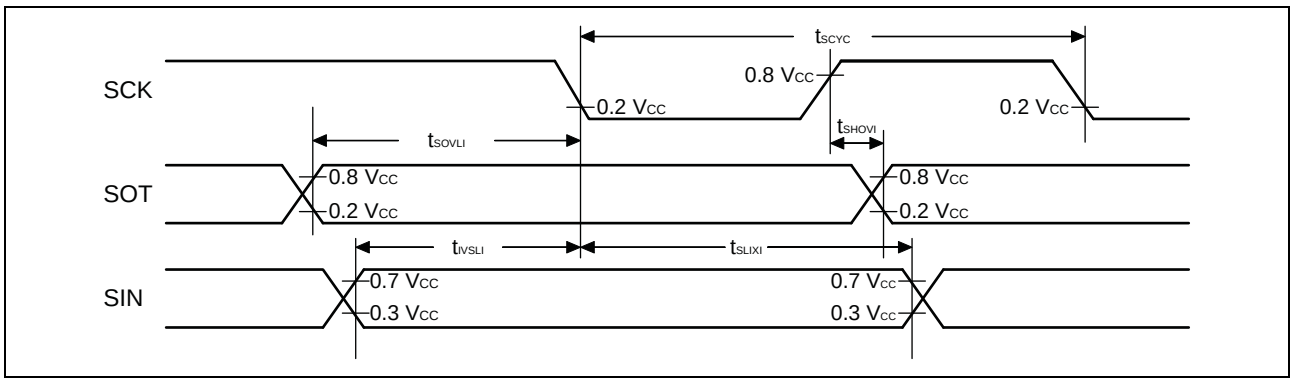
($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK | Internal clock operation output pin: $C_L$ = 80 pF + 1 TTL | 5 $t_{MCLK}$*3 | — | ns |
| SCK↑ → SOT delay time | $t_{SHOVI}$ | SCK, SOT | | –50 | +50 | ns |
| Valid SIN → SCK↓ | $t_{IVSLI}$ | SCK, SIN | | $t_{MCLK}$*3 + 80 | — | ns |
| SCK↓→ valid SIN hold time | $t_{SLIXI}$ | SCK, SIN | | 0 | — | ns |
| SOT → SCK↓delay time | $t_{SOVLI}$ | SCK, SOT | | 3$t_{MCLK}$*3 – 70 | — | ns |

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “(2) Source Clock/Machine Clock” for $t_{MCLK}$.



**Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is enabled*2. (ESCR register : SCES bit = 1, ECCR register : SCDE bit = 1)**

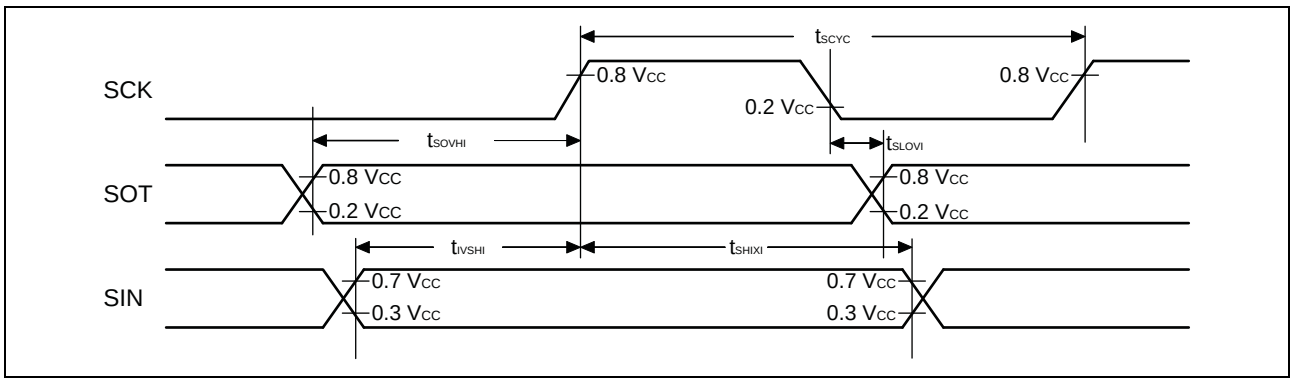
($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK | Internal clock operation output pin: $C_L$ = 80 pF + 1 TTL | 5 $t_{MCLK}$*3 | — | ns |
| SCK↓ → SOT delay time | $t_{SLOVI}$ | SCK, SOT | | –50 | +50 | ns |
| Valid SIN → SCK↑ | $t_{IVSHI}$ | SCK, SIN | | $t_{MCLK}$*3 + 80 | — | ns |
| SCK↑ → valid SIN hold time | $t_{SHIXI}$ | SCK, SIN | | 0 | — | ns |
| SOT → SCK↑delay time | $t_{SOVHI}$ | SCK, SOT | | 3$t_{MCLK}$*3 – 70 | — | ns |

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “(2) Source Clock/Machine Clock” for $t_{MCLK}$.



### (7) Low-voltage Detection

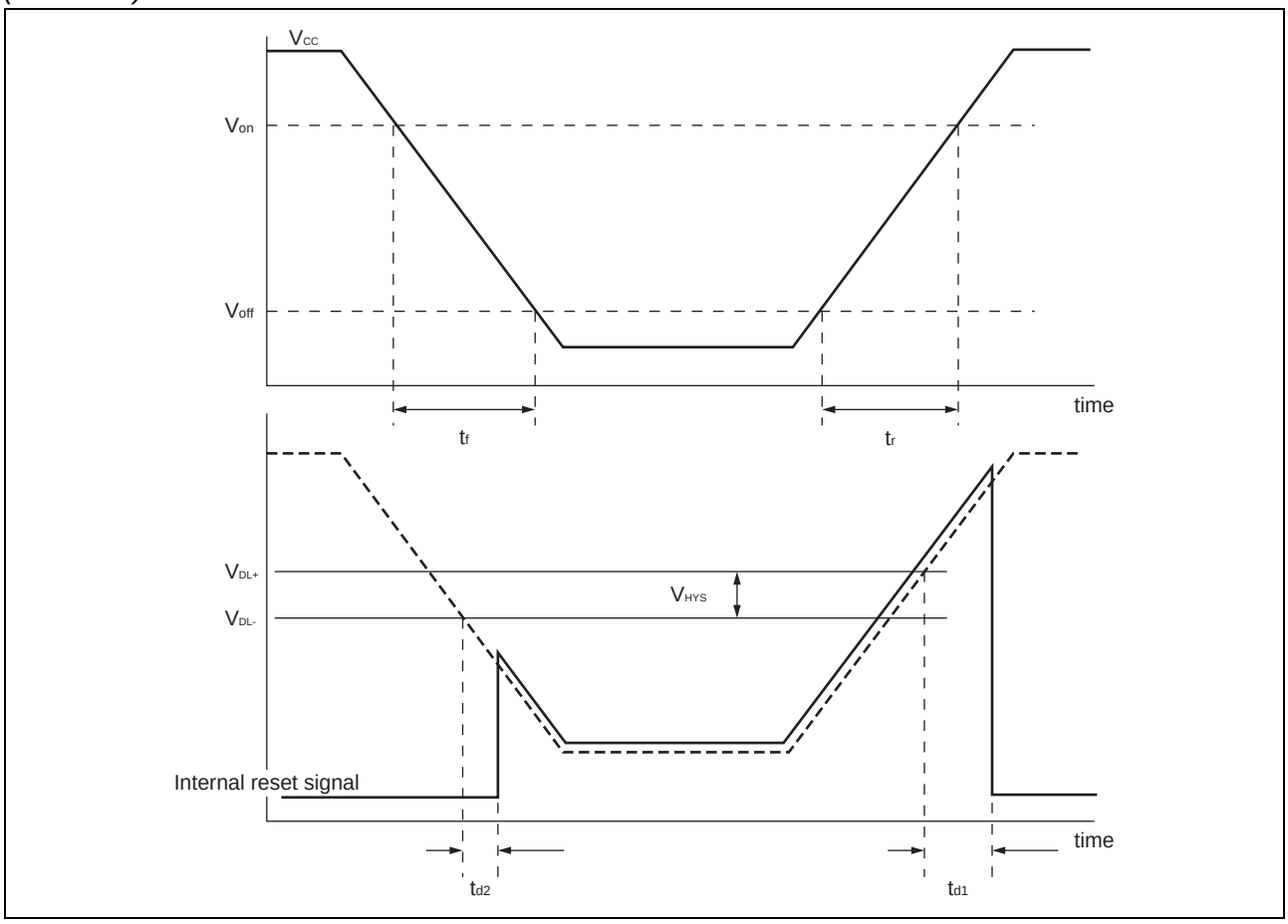
($V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Release voltage* | $V_{DL+}$ | 2.52 | 2.7 | 2.88 | V | At power supply rise |
| | | 2.61 | 2.8 | 2.99 | | |
| | | 2.89 | 3.1 | 3.31 | | |
| | | 3.08 | 3.3 | 3.52 | | |
| Detection voltage* | $V_{DL-}$ | 2.43 | 2.6 | 2.77 | V | At power supply fall |
| | | 2.52 | 2.7 | 2.88 | | |
| | | 2.80 | 3 | 3.20 | | |
| | | 2.99 | 3.2 | 3.41 | | |
| Hysteresis width | $V_{HYS}$ | — | — | 100 | mV | |
| Power supply start voltage | $V_{off}$ | — | — | 2.3 | V | |
| Power supply end voltage | $V_{on}$ | 4.9 | — | — | V | |
| Power supply voltage change time (at power supply rise) | $t_r$ | 650 | — | — | µs | Slope of power supply that the reset release signal generates within the rating ($V_{DL+}$) |
| Power supply voltage change time (at power supply fall) | $t_f$ | 650 | — | — | µs | Slope of power supply that the reset release signal generates within the rating ($V_{DL-}$) |
| Reset release delay time | $t_{d1}$ | — | — | 30 | µs | |
| Reset detection delay time | $t_{d2}$ | — | — | 30 | µs | |
| LVD reset threshold voltage transition stabilization time | $t_{stb}$ | 10 | — | — | µs | |

*: After the LVD reset is enabled by the LVD reset circuit control register (LVDCC), the release voltage and the detection voltage can be selected by using the LVD reset voltage selection ID register (LVDR) in the low-voltage detection reset circuit. For details of the LVDCC register and the LVDR register, refer to “CHAPTER 17 LOW-VOLTAGE DETECTION RESET CIRCUIT” in “New 8FX MB95810K Series Hardware Manual”.

*(Continued)*

*(Continued)*


$V_{CC}$
$V_{on}$
$V_{off}$
time
$t_f$
$t_r$
$V_{DL+}$
$V_{DL-}$
$V_{HYS}$
Internal reset signal
time
$t_{d2}$
$t_{d1}$

### (8) I²C Bus Interface Timing

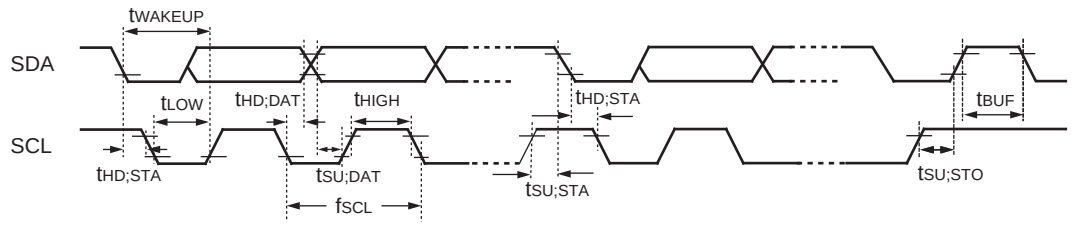
($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Standard-mode | | Fast-mode | | |
| | | | | Min | Max | Min | Max | |
| SCL clock frequency | $f_{SCL}$ | SCL | R = 1.7 kΩ, C = 50 pF*1 | 0 | 100 | 0 | 400 | kHz |
| (Repeated) START condition hold time SDA ↓ → SCL ↓ | $t_{HD;STA}$ | SCL, SDA | | 4.0 | — | 0.6 | — | µs |
| SCL clock “L” width | $t_{LOW}$ | SCL | | 4.7 | — | 1.3 | — | µs |
| SCL clock “H” width | $t_{HIGH}$ | SCL | | 4.0 | — | 0.6 | — | µs |
| (Repeated) START condition setup time SCL ↑ → SDA ↓ | $t_{SU;STA}$ | SCL, SDA | | 4.7 | — | 0.6 | — | µs |
| Data hold time SCL ↓ → SDA ↓↑ | $t_{HD;DAT}$ | SCL, SDA | | 0 | 3.45*2 | 0 | 0.9*3 | µs |
| Data setup time SDA ↓↑ → SCL ↑ | $t_{SU;DAT}$ | SCL, SDA | | 0.25 | — | 0.1 | — | µs |
| STOP condition setup time SCL ↑ → SDA ↑ | $t_{SU;STO}$ | SCL, SDA | | 4 | — | 0.6 | — | µs |
| Bus free time between STOP condition and START condition | $t_{BUF}$ | SCL, SDA | | 4.7 | — | 1.3 | — | µs |

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

*2: The maximum $t_{HD;DAT}$ in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at “L” ($t_{LOW}$) does not extend.

*3: A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, provided that the condition of $t_{SU;DAT} \geq 250$ ns is fulfilled.




*(Continued)*

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value*2 | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCL clock “L” width | $t_{LOW}$ | SCL | R = 1.7 kΩ, C = 50 pF*1 | (2 + nm/2)$t_{MCLK}$ – 20 | — | ns | Master mode |
| SCL clock “H” width | $t_{HIGH}$ | SCL | | (nm/2)$t_{MCLK}$ – 20 | (nm/2)$t_{MCLK}$ + 20 | ns | Master mode |
| START condition hold time | $t_{HD;STA}$ | SCL, SDA0 | | (-1 + nm/2)$t_{MCLK}$ – 20 | (-1 + nm)$t_{MCLK}$ + 20 | ns | Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied. |
| STOP condition setup time | $t_{SU;STO}$ | SCL, SDA | | (1 + nm/2)$t_{MCLK}$ – 20 | (1 + nm/2)$t_{MCLK}$ + 20 | ns | Master mode |
| START condition setup time | $t_{SU;STA}$ | SCL, SDA | | (1 + nm/2)$t_{MCLK}$ – 20 | (1 + nm/2)$t_{MCLK}$ + 20 | ns | Master mode |
| Bus free time between STOP condition and START condition | $t_{BUF}$ | SCL, SDA | | (2 nm + 4) $t_{MCLK}$ – 20 | — | ns | |
| Data hold time | $t_{HD;DAT}$ | SCL, SDA | | 3 $t_{MCLK}$ – 20 | — | ns | Master mode |
| Data setup time | $t_{SU;DAT}$ | SCL, SDA | | (-2 + nm/2) $t_{MCLK}$ – 20 | (-1 + nm/2) $t_{MCLK}$ + 20 | ns | Master mode It is assumed that “L” of SCL is not extended. The minimum value is applied to the first bit of continuous data. Otherwise, the maximum value is applied. |
| Setup time between clearing interrupt and SCL rising | $t_{SU;INT}$ | SCL | | (nm/2) $t_{MCLK}$ – 20 | (1 + nm/2) $t_{MCLK}$ + 20 | ns | The minimum value is applied to the interrupt at the ninth SCL↓. The maximum value is applied to the interrupt at the eighth SCL↓. |
| SCL clock “L” width | $t_{LOW}$ | SCL | | 4 $t_{MCLK}$ – 20 | — | ns | At reception |
| SCL clock “H” width | $t_{HIGH}$ | SCL | | 4 $t_{MCLK}$ – 20 | — | ns | At reception |

*(Continued)*

*(Continued)*

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value*2 | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| START condition detection | $t_{HD;STA}$ | SCL, SDA | R = 1.7 kΩ, C = 50 pF*1 | 2 $t_{MCLK}$ – 20 | — | ns | No START condition is detected when 1 $t_{MCLK}$ is used at reception. |
| STOP condition detection | $t_{SU;STO}$ | SCL, SDA | | 2 $t_{MCLK}$ – 20 | — | ns | No STOP condition is detected when 1 $t_{MCLK}$ is used at reception. |
| RESTART condition detection condition | $t_{SU;STA}$ | SCL, SDA | | 2 $t_{MCLK}$ – 20 | — | ns | No RESTART condition is detected when 1 $t_{MCLK}$ is used at reception. |
| Bus free time | $t_{BUF}$ | SCL, SDA | | 2 $t_{MCLK}$ – 20 | — | ns | At reception |
| Data hold time | $t_{HD;DAT}$ | SCL, SDA | | 2 $t_{MCLK}$ – 20 | — | ns | At slave transmission mode |
| Data setup time | $t_{SU;DAT}$ | SCL, SDA | | $t_{LOW}$ – 3 $t_{MCLK}$ – 20 | — | ns | At slave transmission mode |
| Data hold time | $t_{HD;DAT}$ | SCL, SDA | | 0 | — | ns | At reception |
| Data setup time | $t_{SU;DAT}$ | SCL, SDA | | $t_{MCLK}$ – 20 | — | ns | At reception |
| SDA↓ → SCL↑ (with wakeup function in use) | $t_{WAKEUP}$ | SCL, SDA | | Oscillation stabilization wait time +2 $t_{MCLK}$ – 20 | — | ns | |

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA0 lines.

*2: • See “(2) Source Clock/Machine Clock” for $t_{MCLK}$.
- m represents the CS[4:3] bits in the I²C clock control register (ICCR0).
- n represents the CS[2:0] bits in the I²C clock control register (ICCR0).
- The actual timing of the I²C bus interface is determined by the values of m and n set by the machine clock ($t_{MCLK}$) and the CS[4:0] bits in the ICCR0 register.
- Standard-mode:
  m and n can be set to values in the following range: 0.9 MHz < $t_{MCLK}$ (machine clock) < 16.25 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 0.9 MHz < $t_{MCLK}$ ≤ 1 MHz
  (m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4) : 0.9 MHz < $t_{MCLK}$ ≤ 2 MHz
  (m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8) : 0.9 MHz < $t_{MCLK}$ ≤ 4 MHz
  (m, n) = (1, 98), (5, 22), (6, 22), (7, 22) : 0.9 MHz < $t_{MCLK}$ ≤ 10 MHz
  (m, n) = (8, 22) : 0.9 MHz < $t_{MCLK}$ ≤ 16.25 MHz
- Fast-mode:
  m and n can be set to values in the following range: 3.3 MHz < $t_{MCLK}$ (machine clock) < 16.25 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 3.3 MHz < $t_{MCLK}$ ≤ 4 MHz
  (m, n) = (1, 22), (5, 4) : 3.3 MHz < $t_{MCLK}$ ≤ 8 MHz
  (m, n) = (1, 38), (6, 4), (7, 4), (8, 4) : 3.3 MHz < $t_{MCLK}$ ≤ 10 MHz
  (m, n) = (5, 8) : 3.3 MHz < $t_{MCLK}$ ≤ 16.25 MHz

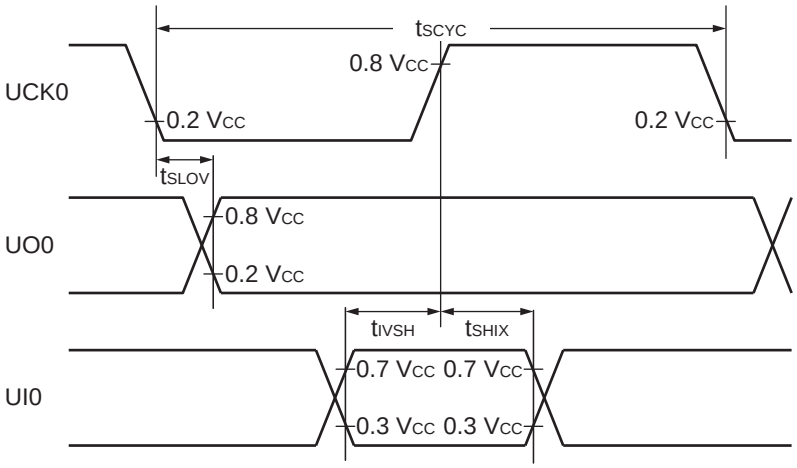
### (9) UART/SIO, Serial I/O Timing

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

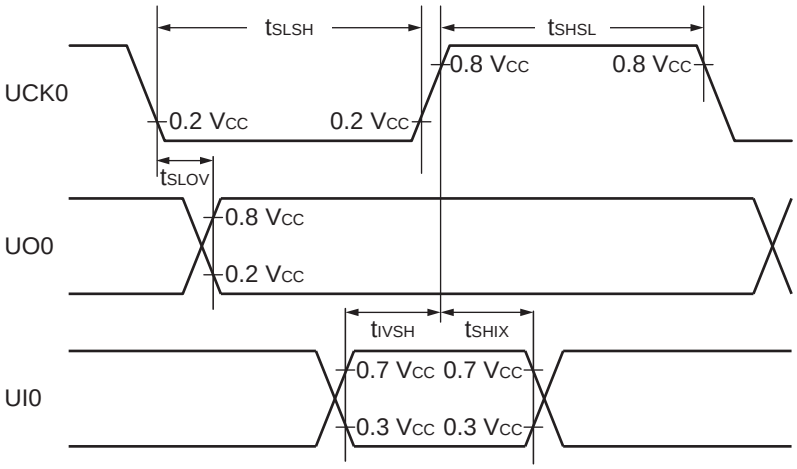
| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | UCK0 | Internal clock operation | 4 $t_{MCLK}$* | — | ns |
| UCK ↓ → UO time | $t_{SLOV}$ | UCK0, UO0 | | –190 | +190 | ns |
| Valid UI → UCK ↑ | $t_{IVSH}$ | UCK0, UI0 | | 2 $t_{MCLK}$* | — | ns |
| UCK ↑ → valid UI hold time | $t_{SHIX}$ | UCK0, UI0 | | 2 $t_{MCLK}$* | — | ns |
| Serial clock “H” pulse width | $t_{SHSL}$ | UCK0 | External clock operation | 4 $t_{MCLK}$* | — | ns |
| Serial clock “L” pulse width | $t_{SLSH}$ | UCK0 | | 4 $t_{MCLK}$* | — | ns |
| UCK ↓ → UO time | $t_{SLOV}$ | UCK0, UO0 | | — | 190 | ns |
| Valid UI → UCK ↑ | $t_{IVSH}$ | UCK0, UI0 | | 2 $t_{MCLK}$* | — | ns |
| UCK ↑ → valid UI hold time | $t_{SHIX}$ | UCK0, UI0 | | 2 $t_{MCLK}$* | — | ns |

*: See “(2) Source Clock/Machine Clock” for $t_{MCLK}$.

- Internal shift clock mode




- External shift clock mode



### (10) Comparator Timing

($V_{CC}$ = 2.88 V to 5.5 V, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Voltage range | CMP0_P, CMP0_N, CMP1_P, CMP1_N | 0 | — | $V_{CC}$ – 1.3 | V | |
| Offset voltage | CMP0_P, CMP0_N, CMP1_P, CMP1_N | –15 | — | +15 | mV | |
| Delay time | CMP0_O, CMP1_O | — | 650 | 1200 | ns | Overdrive 5 mV |
| | | — | 140 | 420 | ns | Overdrive 50 mV |
| Power down delay | CMP0_O, CMP1_O | — | — | 1200 | ns | Power down recovery<br>PD: 1 → 0 |
| Power up stabilization wait time | CMP0_O, CMP1_O | — | — | 1200 | ns | Output stabilization time at power up |

### (11) BGR for Comparator

($V_{CC}$ = 2.88 V to 5.5 V, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Power up stabilization wait time | — | — | — | 150 | µs | Load: 10 pF |
| Output voltage | VBGR | 1.1495 | 1.21 | 1.2705 | V | |

## 5. A/D Converter

### (1) A/D Converter Electrical Characteristics

($AV_{CC}$ = $V_{CC}$ = 2.7 V to 5.5 V, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

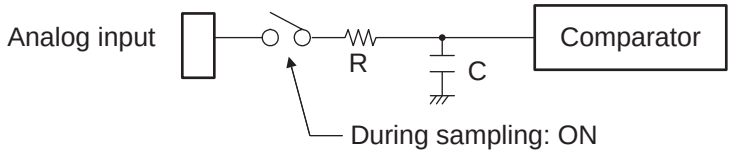
| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Resolution | — | — | — | 10 | bit | |
| Total error | | –3 | — | +3 | LSB | |
| Linearity error | | –2.5 | — | +2.5 | LSB | |
| Differential linearity error | | –1.9 | — | +1.9 | LSB | |
| Zero transition voltage | $V_{0T}$ | $AV_{SS}$ – 7.2 LSB | $AV_{SS}$ + 0.5 LSB | $AV_{SS}$ + 8.2 LSB | V | |
| Full-scale transition voltage | $V_{FST}$ | AVR – 6.2 LSB | AVR – 1.5 LSB | AVR + 9.2 LSB | V | |
| Compare time | — | 3 | — | 10 | µs | 2.7 V ≤ $AV_{CC}$ ≤ 5.5 V |
| Sampling time | — | 0.941 | — | ∞ | µs | 2.7 V ≤ $AV_{CC}$ ≤ 5.5 V, with external impedance < 3.3 kΩ and external capacitance = 10 pF |
| Analog input current | $I_{AIN}$ | –0.3 | — | +0.3 | µA | |
| Analog input voltage | $V_{AIN}$ | $AV_{SS}$ | — | AVR | V | |
| Reference voltage | — | $AV_{CC}$ – 0.1 | — | $AV_{CC}$ | V | Voltage applied to the AVR pin |

### (2) Notes on Using A/D Converter

- External impedance of analog input and its sampling time

  The A/D converter of has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

- Analog input equivalent circuit

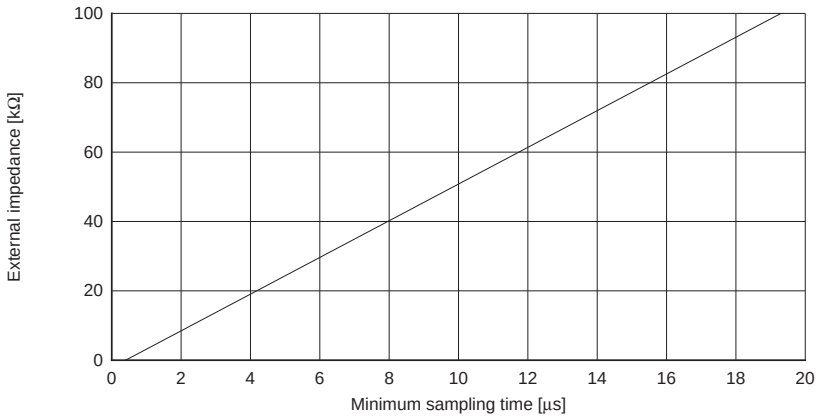



| $V_{CC}$ | R | C |
|---|---|---|
| 4.5 V ≤ $AV_{CC}$ ≤ 5.5 V | 1.45 kΩ (Max) | 14.89 pF (Max) |
| 2.7 V ≤ $AV_{CC}$ < 4.5 V | 2.7 kΩ (Max) | 14.89 pF (Max) |

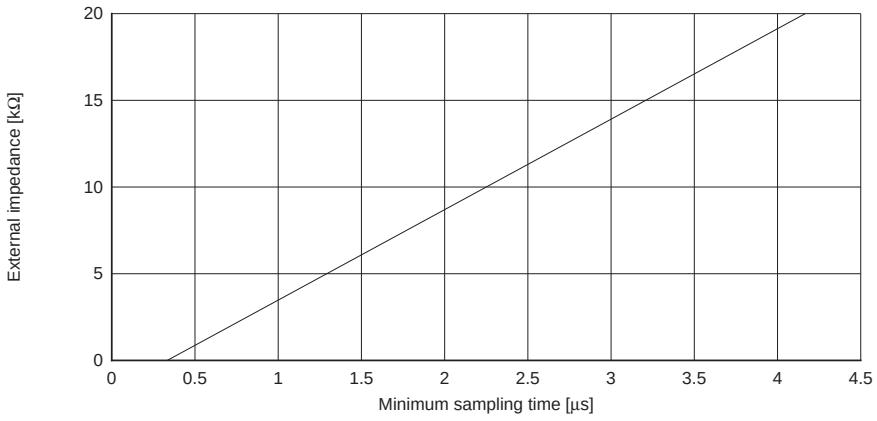
Note: The values are reference values.

- Relationship between external impedance and minimum sampling time

[External impedance = 0 kΩ to 100 kΩ]




[External impedance = 0 kΩ to 20 kΩ]



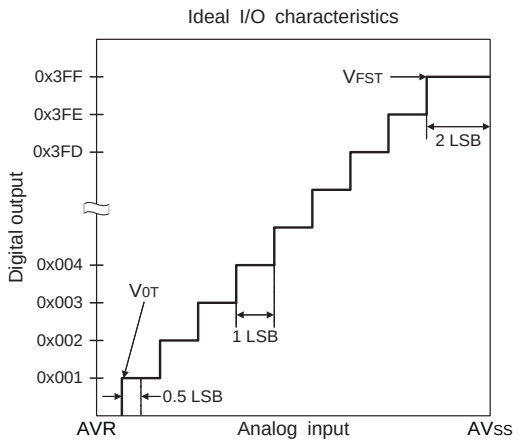

Note: External capacitance = 10 pF

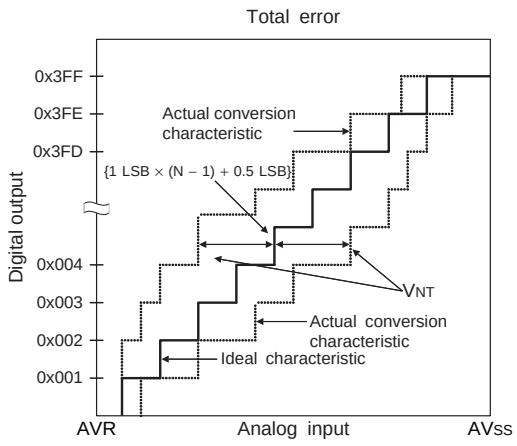
- A/D conversion error

  As |AVR – $AV_{SS}$| decreases, the A/D conversion error increases proportionately.

**(3) Definitions of A/D Converter Terms**

- Resolution
  It indicates the level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into $2^{10}$ = 1024.
- Linearity error (unit: LSB)
  It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point (“0000000000” ← → “0000000001”) of a device to the full-scale transition point (“1111111111” ← → “1111111110”) of the same device.
- Differential linear error (unit: LSB)
  It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.
- Total error (unit: LSB)
  It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.




$$1\ \text{LSB} = \frac{\text{AVR} - \text{AVSS}}{1024}\ \text{V}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ \text{LSB}$$

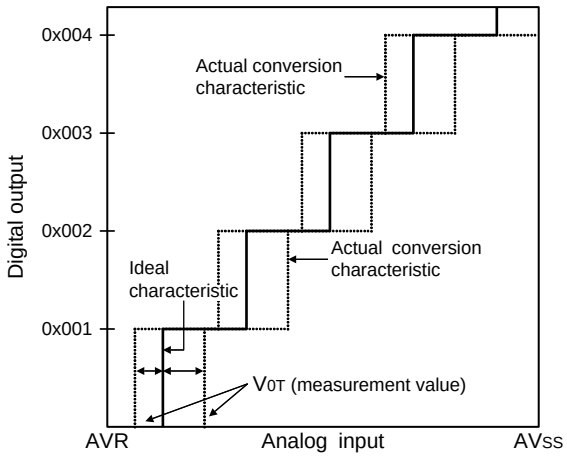
N : A/D converter digital output value

$V_{NT}$ : Voltage at which the digital output transits from 0x(N – 1) to 0xN

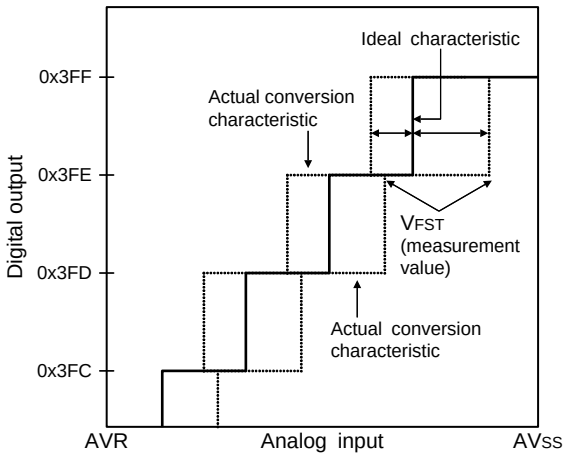
*(Continued)*

*(Continued)*

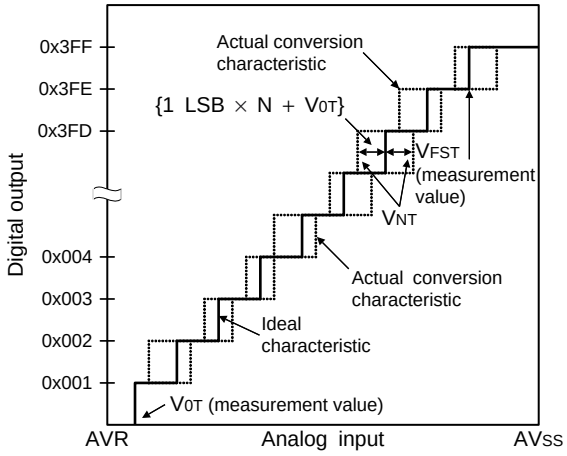
Zero transition error



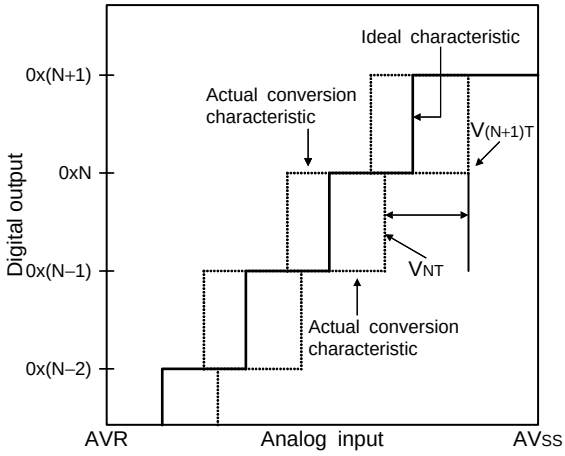

Full-scale transition error




Linearity error




Differential linearity error




$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{0T}\}}{1\ \text{LSB}}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

N : A/D converter digital output value

$V_{NT}$ : Voltage at which the digital output transits from 0x(N – 1) to 0xN

$V_{0T}$ (ideal value) = AVR + 0.5 LSB [V]

$V_{FST}$ (ideal value) = $AV_{SS}$ – 2 LSB [V]

### 6. Flash Memory Program/Erase Characteristics

| Parameter | Value | | | Unit | Remarks |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| Sector erase time (2 Kbyte sector) | — | 0.3*1 | 1.6*2 | s | The time of writing “0x00” prior to erasure is excluded. |
| Sector erase time (32 Kbyte sector) | — | 0.6*1 | 3.1*2 | s | The time of writing “0x00” prior to erasure is excluded. |
| Byte writing time | — | 17 | 272 | µs | System-level overhead is excluded. |
| Program/erase cycle | 100000 | — | — | cycle | |
| Power supply voltage at program/erase | 2.4 | — | 5.5 | V | |
| Flash memory data retention time | 20*3 | — | — | year | Average $T_A$ = +85 °C<br>Number of program/erase cycles: 1000 or below |
| | 10*3 | — | — | | Average $T_A$ = +85 °C<br>Number of program/erase cycles: 1001 to 10000 inclusive |
| | 5*3 | — | — | | Average $T_A$ = +85 °C<br>Number of program/erase cycles: 10001 or above |

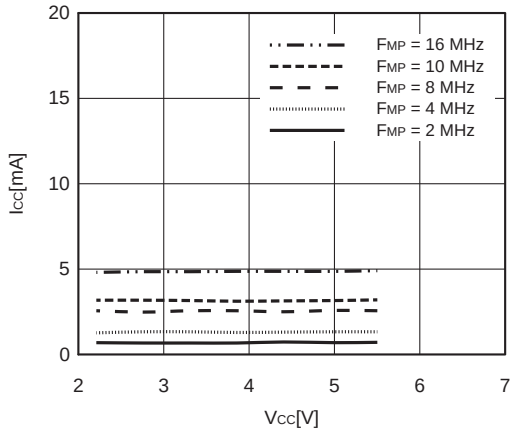
*1: $V_{CC}$ = 5.5 V, $T_A$ = +25 °C, 0 cycle
*2: $V_{CC}$ = 2.4 V, $T_A$ = +85 °C, 100000 cycles
*3: These values were converted from the result of a technology reliability assessment. (These values were converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85 °C.)

## ■ SAMPLE CHARACTERISTICS

• Power supply current temperature characteristics

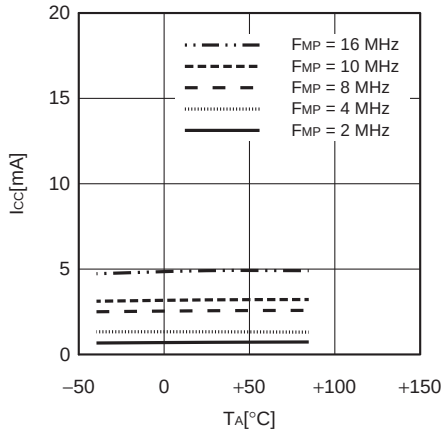
$I_{CC}$ – $V_{CC}$

$T_A$ = +25 °C, $F_{MP}$ = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



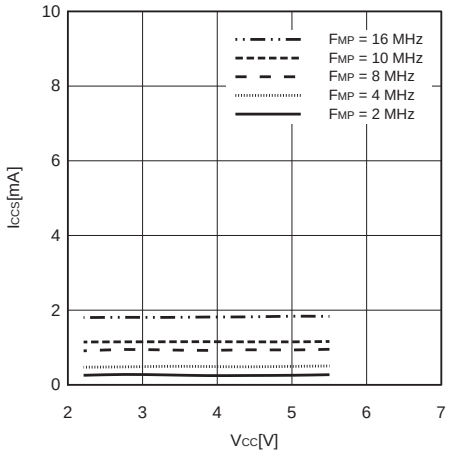

$I_{CC}$ – $T_A$

$V_{CC}$ = 5.5 V, $F_{MP}$ = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



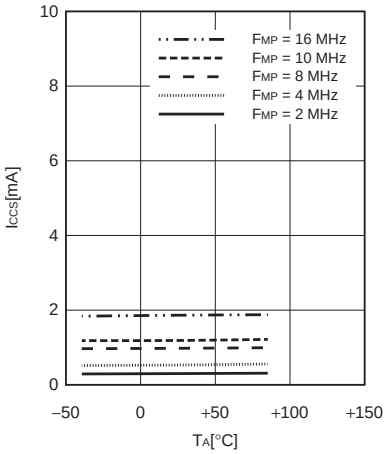

$I_{CCS}$ – $V_{CC}$

$T_A$ = +25 °C, $F_{MP}$ = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



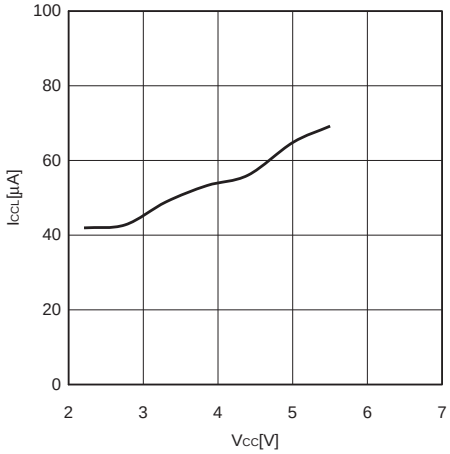

$I_{CCS}$ – $T_A$

$V_{CC}$ = 5.5 V, $F_{MP}$ = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



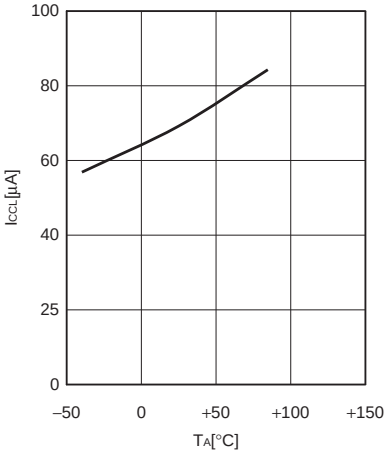

$I_{CCL}$ – $V_{CC}$

$T_A$ = +25 °C, $F_{MPL}$ = 16 kHz (divided by 2)
Subclock mode with the external clock operating




$I_{CCL}$ – $T_A$

$V_{CC}$ = 5.5 V, $F_{MPL}$ = 16 kHz (divided by 2)
Subclock mode with the external clock operating

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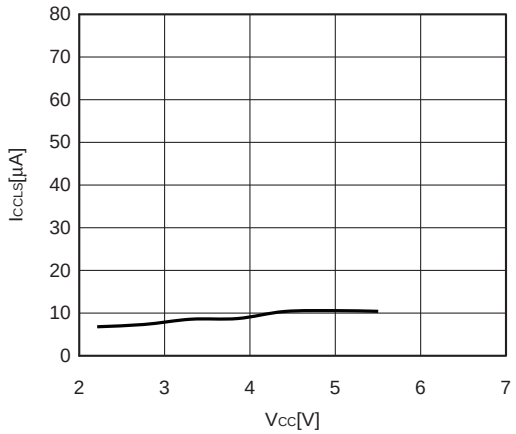
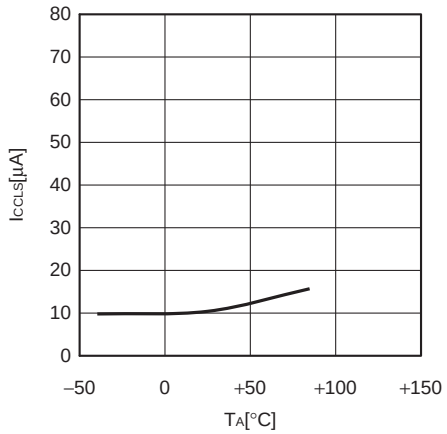
$I_{CCLS}$ – $V_{CC}$

$T_A$ = +25 °C, $F_{MPL}$ = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



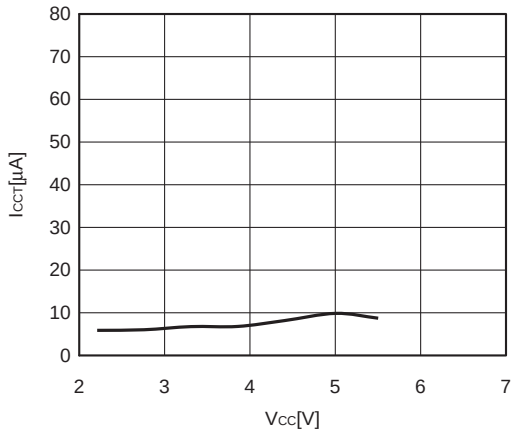

$I_{CCLS}$ – $T_A$

$V_{CC}$ = 5.5 V, $F_{MPL}$ = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



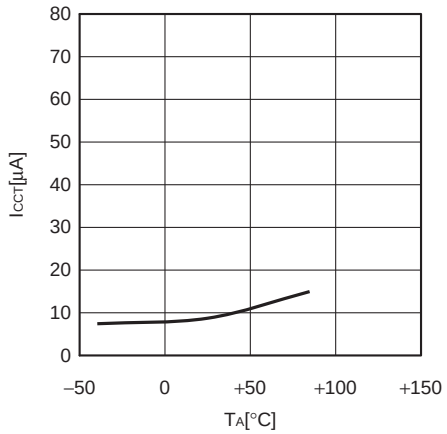

$I_{CCT}$ – $V_{CC}$

$T_A$ = +25 °C, $F_{MPL}$ = 16 kHz (divided by 2)
Watch mode with the external clock operating



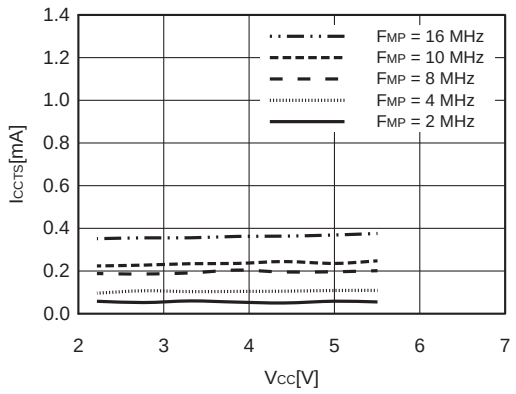

$I_{CCT}$ – $T_A$

$V_{CC}$ = 5.5 V, $F_{MPL}$ = 16 kHz (divided by 2)
Watch mode with the external clock operating



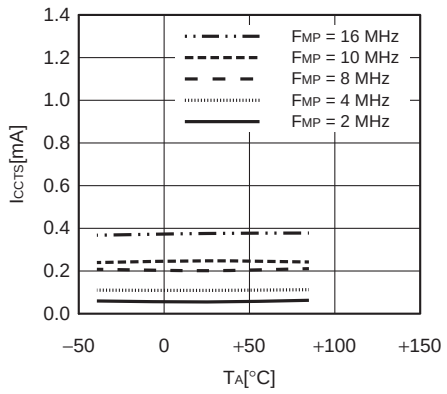

$I_{CCTS}$ – $V_{CC}$

$T_A$ = +25 °C, $F_{MP}$ = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



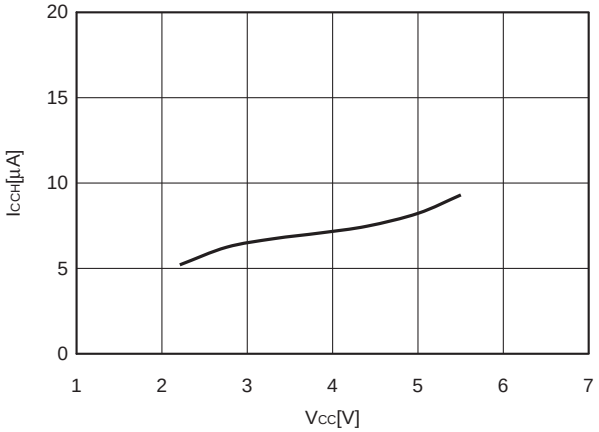

$I_{CCTS}$ – $T_A$

$V_{CC}$ = 5.5 V, $F_{MP}$ = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating

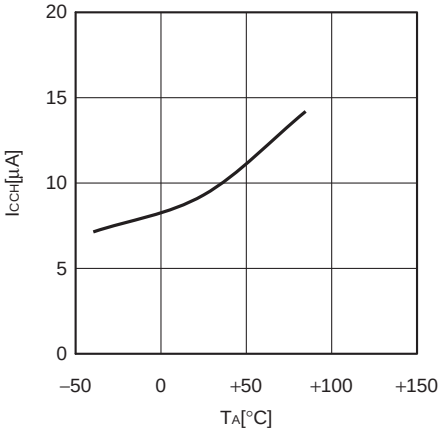



*(Continued)*

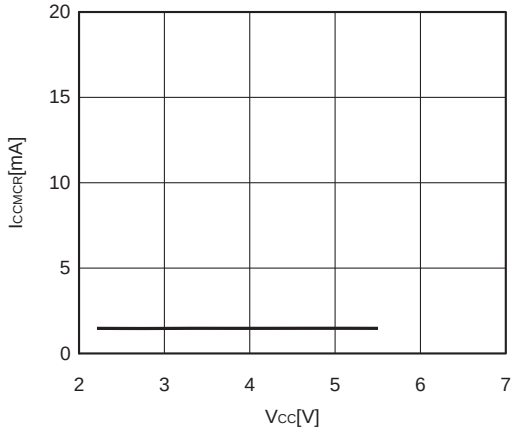
$I_{CCH}$ – $V_{CC}$
$T_A$ = +25 °C, $F_{MPL}$ = (stop)
Substop mode with the external clock stopping



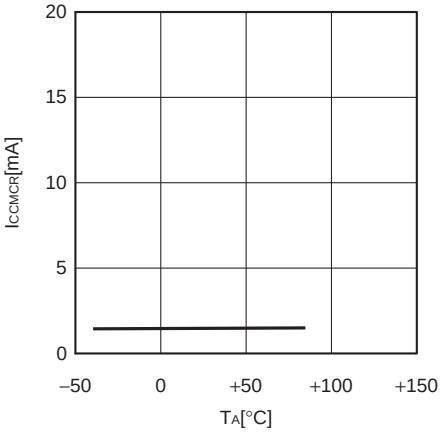

$I_{CCH}$ – $T_A$
$V_{CC}$ = 5.5 V, $F_{MPL}$ = (stop)
Substop mode with the external clock stopping



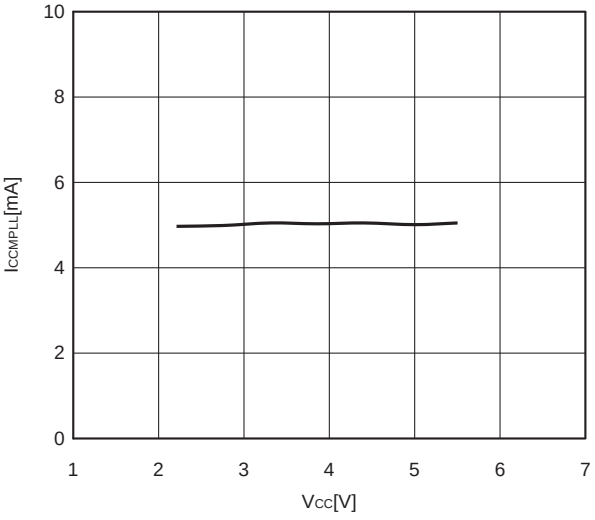

$I_{CCMCR}$ – $V_{CC}$
$T_A$ = +25 °C, $F_{MP}$ = 4 MHz (no division)
Main CR clock mode



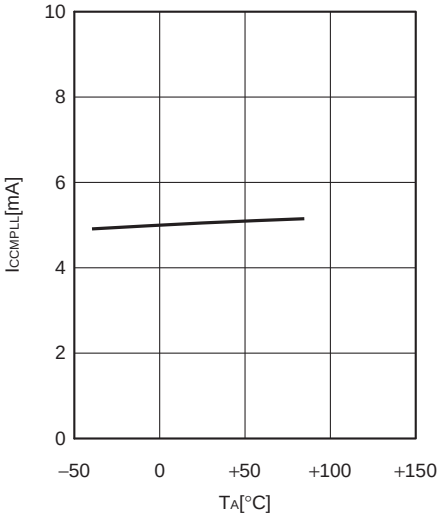

$I_{CCMCR}$ – $T_A$
$V_{CC}$ = 5.5 V, $F_{MP}$ = 4 MHz (no division)
Main CR clock mode




$I_{CCMPLL}$ – $V_{CC}$
$T_A$ = +25 °C, $F_{MP}$ = 16 MHz (PLL multiplication rate: 4)
Main CR PLL clock mode




$I_{CCMPLL}$ – $T_A$
$V_{CC}$ = 5.5 V, $F_{MP}$ = 16 MHz (PLL multiplication rate: 4)
Main CR PLL clock mode

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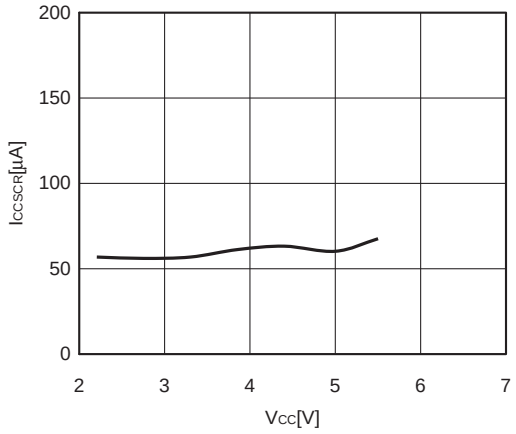
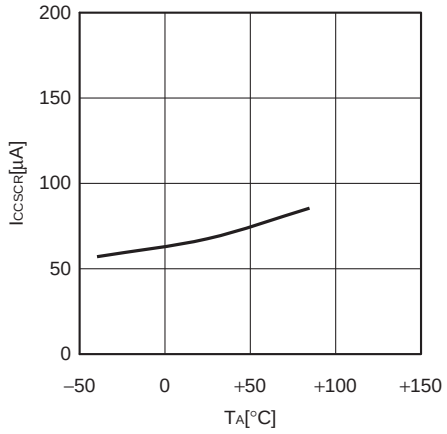
$I_{CCSCR}$ – $V_{CC}$
$T_A$ = +25 °C, $F_{MPL}$ = 50 kHz (divided by 2)
Sub-CR clock mode

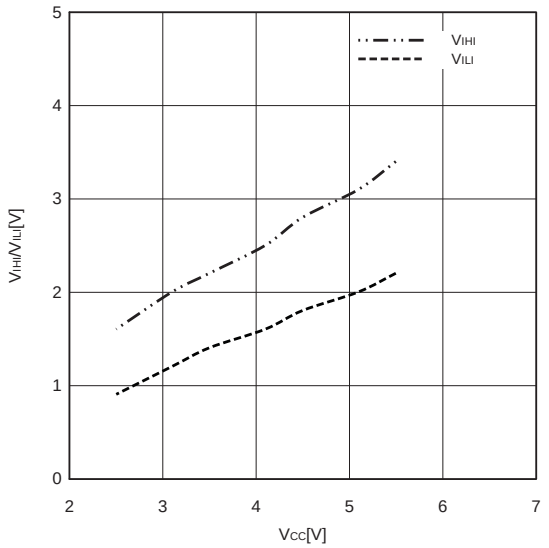



$I_{CCSCR}$ – $T_A$
$V_{CC}$ = 5.5 V, $F_{MPL}$ = 50 kHz (divided by 2)
Sub-CR clock mode

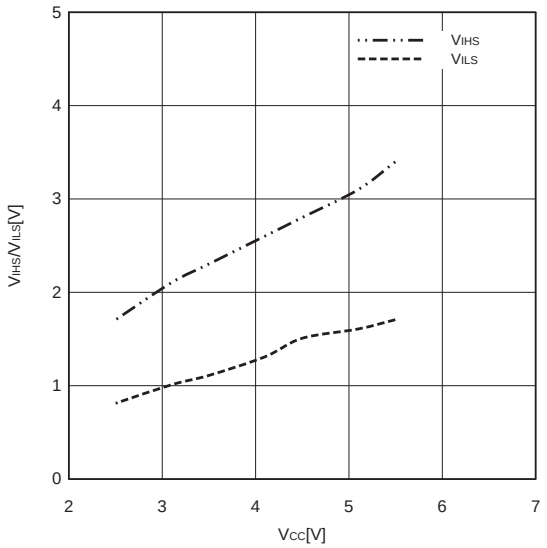


• Input voltage characteristics

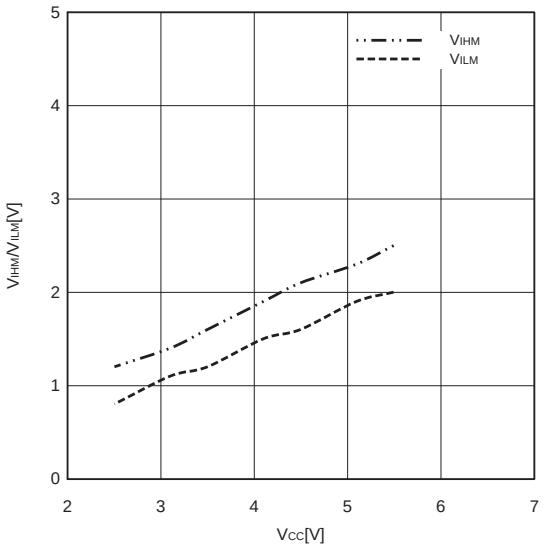
$V_{IHI}$ – $V_{CC}$ and $V_{ILI}$ – $V_{CC}$
$T_A$ = +25 °C




$V_{IHS}$ – $V_{CC}$ and $V_{ILS}$ – $V_{CC}$
$T_A$ = +25 °C

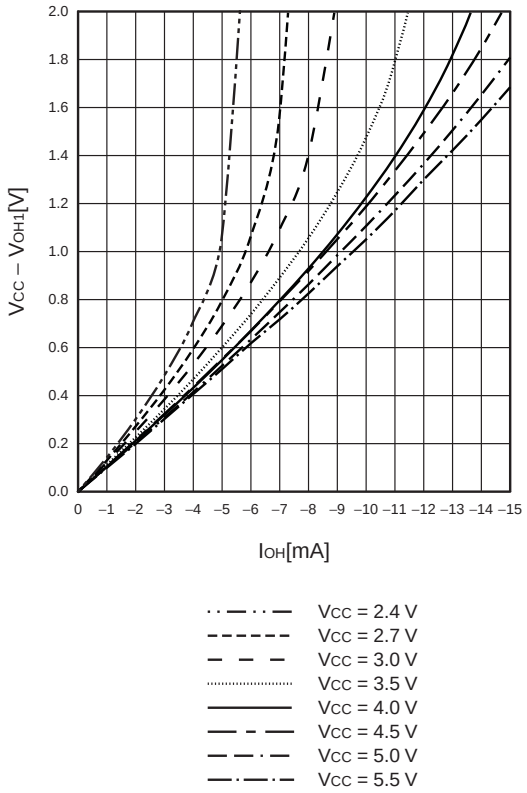



$V_{IHM}$ – $V_{CC}$ and $V_{ILM}$ – $V_{CC}$
$T_A$ = +25 °C

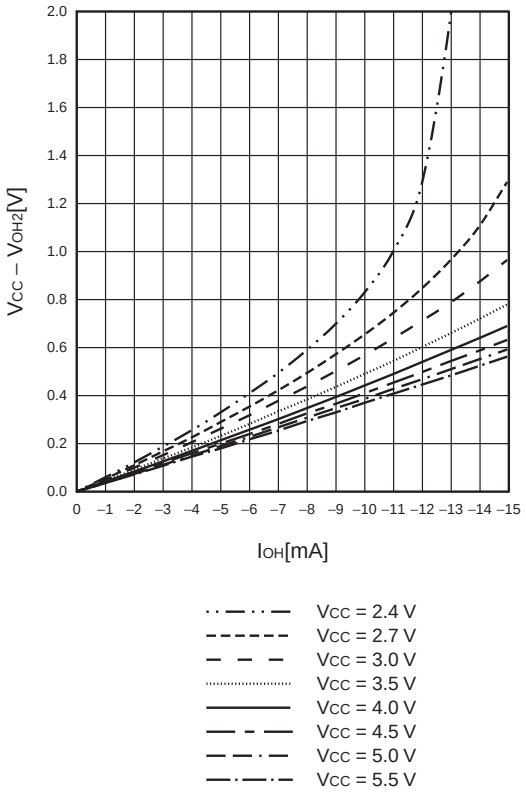


• Output voltage characteristics

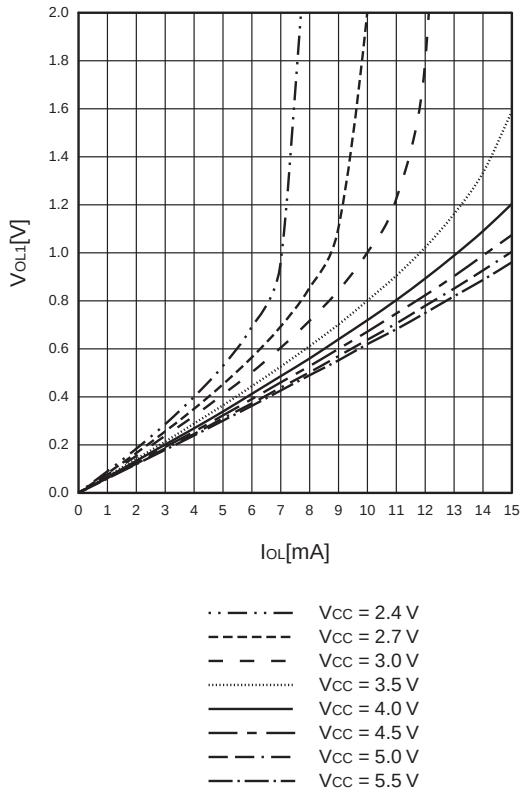
$(V_{CC} - V_{OH1}) - I_{OH}$
$T_A = +25\ °C$



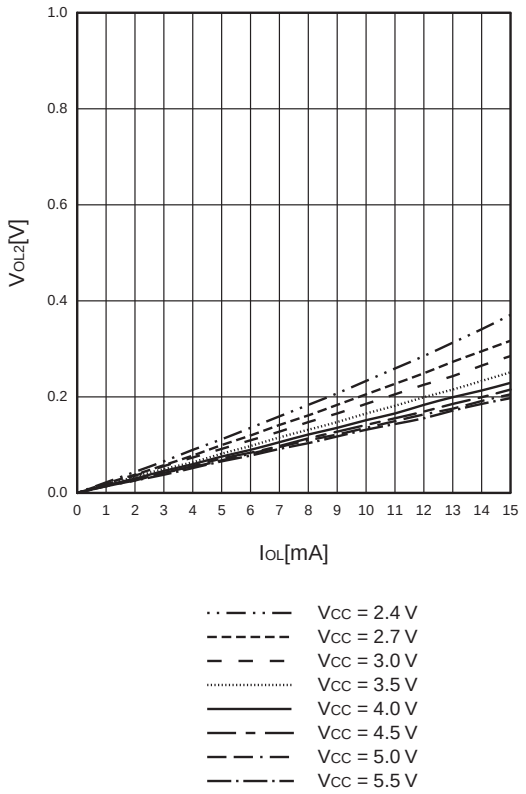

$(V_{CC} - V_{OH2}) - I_{OH}$
$T_A = +25\ °C$



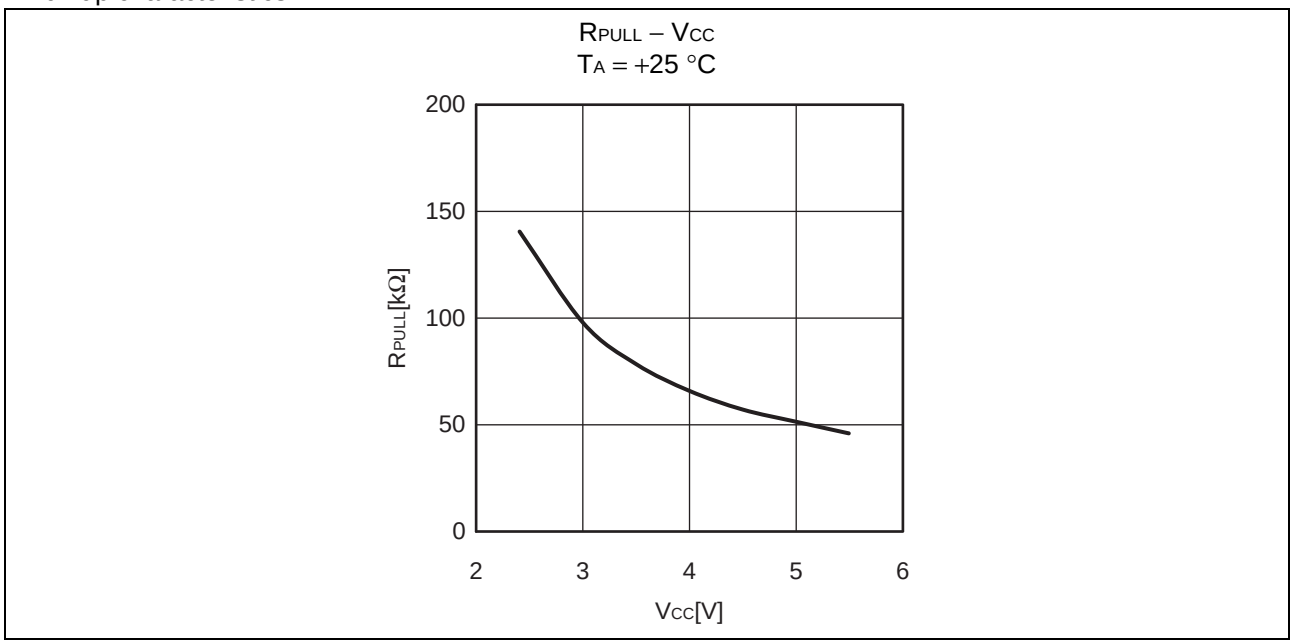

$V_{OL1} - I_{OL}$
$T_A = +25\ °C$




$V_{OL2} - I_{OL}$
$T_A = +25\ °C$



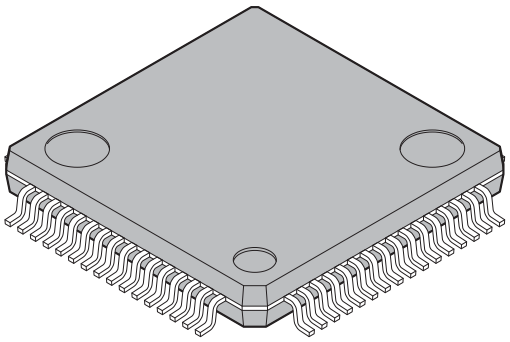
• Pull-up characteristics



## ■ ORDERING INFORMATION

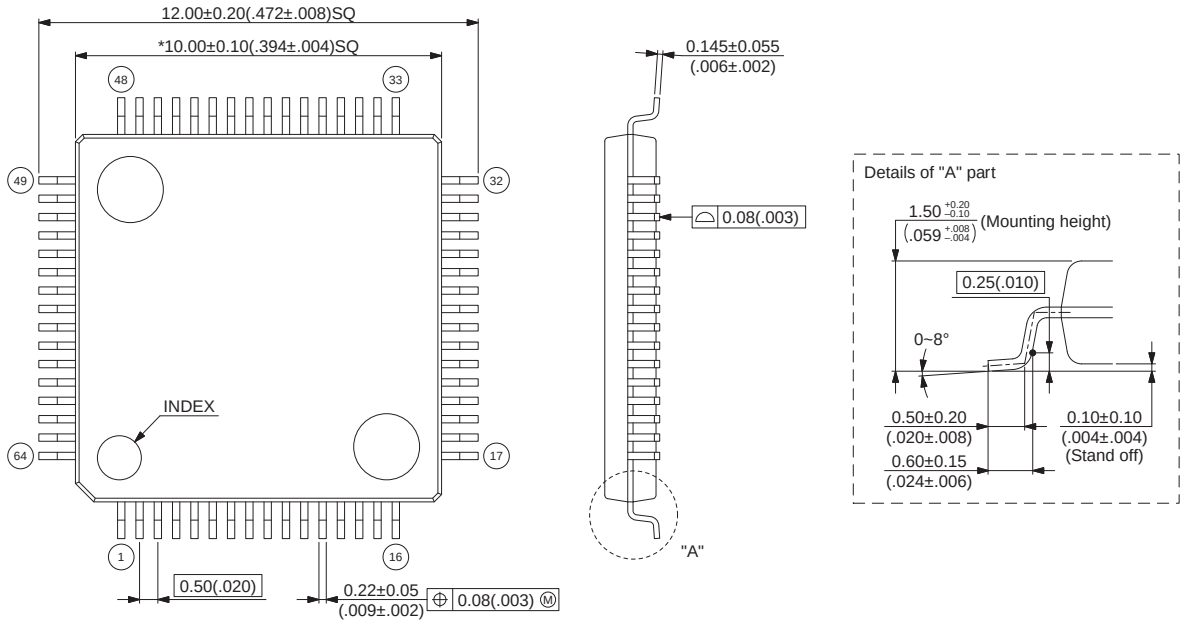
| Part number | Package |
|---|---|
| MB95F814KPMC1-G-SNE2<br>MB95F816KPMC1-G-SNE2<br>MB95F818KPMC1-G-SNE2 | 64-pin plastic LQFP<br>(FPT-64P-M38) |
| MB95F814KPMC-G-SNE2<br>MB95F816KPMC-G-SNE2<br>MB95F818KPMC-G-SNE2 | 64-pin plastic LQFP<br>(FPT-64P-M39) |

## ■ PACKAGE DIMENSION

| 64-pin plastic LQFP | | |
|---|---|---|
|  (FPT-64P-M38) | Lead pitch | 0.50 mm |
| | Package width × package length | 10.00 mm × 10.00 mm |
| | Lead shape | Gullwing |
| | Lead bend direction | Normal bend |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Weight | 0.32 g |

64-pin plastic LQFP
(FPT-64P-M38)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



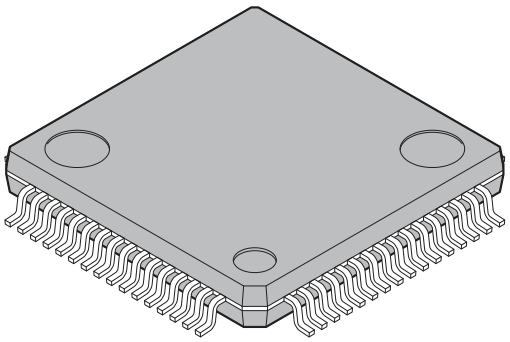



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

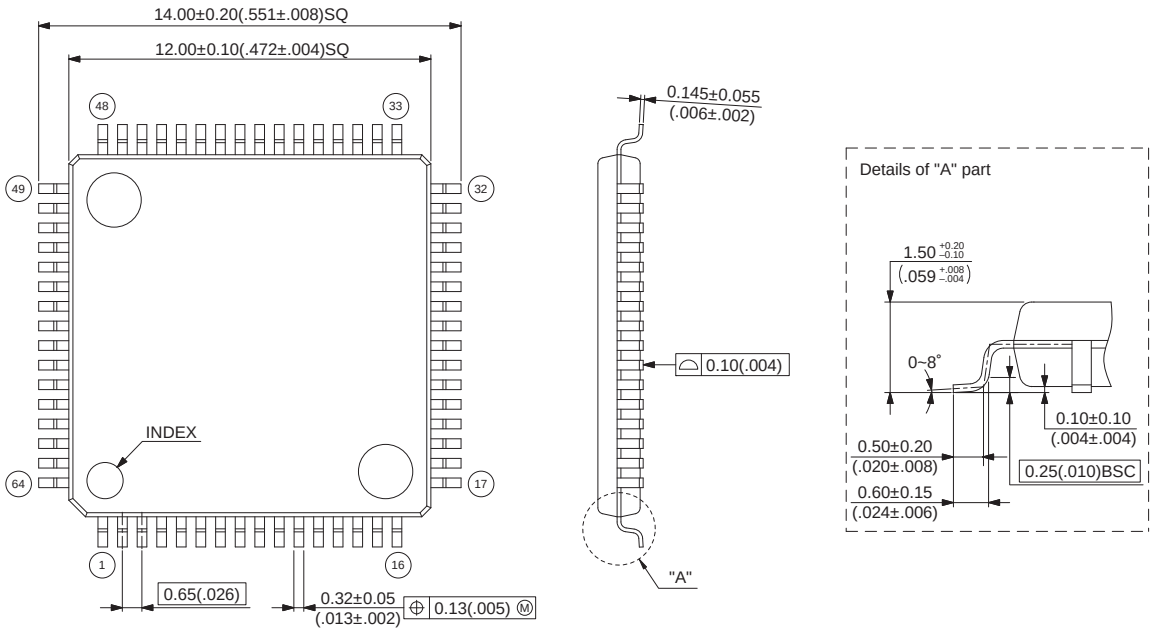
*(Continued)*

*(Continued)*

| 64-pin plastic LQFP | | |
|---|---|---|
|  | Lead pitch | 0.65 mm |
| | Package width × package length | 12.00 mm × 12.00 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Weight | 0.47 g |
| (FPT-64P-M39) | | |

64-pin plastic LQFP
(FPT-64P-M39)

Note 1) Pins width and pins thickness include plating thickness.






Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

## ■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

| Page | Section | Details |
|---|---|---|
| 18 | ■ PIN CONNECTION<br>• DBG pin | Revised details of "• DBG pin". |
| | • $\overline{\text{RST}}$ pin | Revised details of "• $\overline{\text{RST}}$ pin". |
| 19 | • C pin | Corrected the following statement.<br>The bypass capacitor for the $V_{CC}$ pin must have a capacitance larger than $C_S$.<br>→<br>The decoupling capacitor for the $V_{CC}$ pin must have a capacitance equal to or larger than the capacitance of $C_S$. |
| 79 | ■ I/O PORTS<br>11. Port F<br>(4) Port F operations<br>• Operation as an input port | Added the following statement.<br>For a pin shared with other peripheral functions, disable the output of such peripheral functions. |
| 82 | 12. Port G<br>(4) Port G operations<br>• Operation as an input port | Added the following statement.<br>For a pin shared with other peripheral functions, disable the output of such peripheral functions. |
| 89 | ■ ELECTRICAL CHARACTERISTICS<br>2. Recommended Operating Conditions | Corrected the following statement in the remark of the parameter "Decoupling capacitor".<br>The bypass capacitor for the $V_{CC}$ pin must have a capacitance larger than $C_S$.<br>→<br>The decoupling capacitor for the $V_{CC}$ pin must have a capacitance equal to or larger than the capacitance of $C_S$. |
| | | Revised the remark in "• DBG/$\overline{\text{RST}}$/C pins connection diagram". |
| 90 | 3. DC Characteristics | Revised the remark of the parameter "Input leak current (Hi-Z output leak current)".<br>When pull-up resistance is disabled<br>→<br>When the internal pull-up resistor is disabled |
| | | Renamed the parameter "Pull-up resistance" to "Internal pull-up resistor". |
| | | Revised the remark of the parameter "Internal pull-up resistor".<br>When pull-up resistance is enabled<br>→<br>When the internal pull-up resistor is enabled |
| 95 | 4. AC Characteristics<br>(1) Clock Timing | Corrected the pin names of the parameter "Input clock rising time and falling time".<br>X0 → X0, X0A<br>X0, X1 → X0, X1, X0A, X1A |

# MEMO

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